IT6506 Programming Guide

Ver 1.02

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History

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Chap 1 Introduce

The IT6506 is a high-performance DisplayPort 1.1a receiver, fully compliant with DisplayPort **1.1a**,

HDCP 1.3 specifications. The IT6506 with its Deep Color capability (up to 36-bit) ensures robust reception of high-quality uncompressed video content, along with state-of-the-art uncompressed and compressed digital audio content.

Aside from the various video output formats supported, the IT6506 also receives and provides up to 8 channels of I^2S digital audio outputs, with sampling rate up to 192kHz and sample size up to 24 bits, facilitating direct connection to industry-standard low-cost audio DACs. Also, an S/PDIF output is provided to support up to compressed audio of 192kHz frame rate.

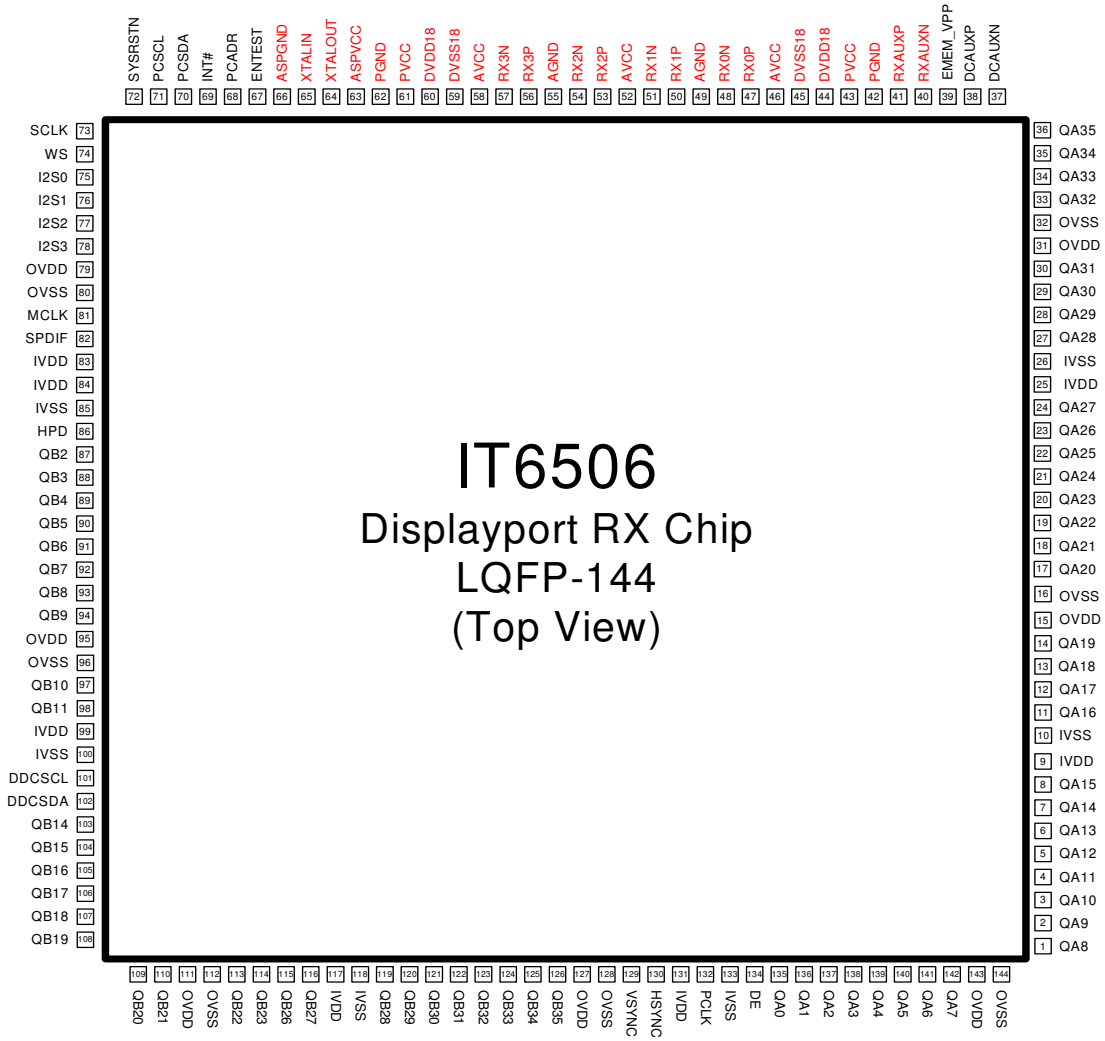
Each IT6506 comes preprogrammed with an unique HDCP key, in compliance with the HDCP 1.3 standard so as to provide secure transmission of high-definition content. Users of the IT6506 need not purchase any HDCP keys or ROMs.

Features

- Compliance with DisplayPort Specification **V1.1a** at **1.62/2.7 Gbps** data rate (Low bit rate/High bit rate)
- Support flexible **1/2/4** lanes configurations; Full **10.8Gbps** data rate support(4 lanes at 2.7Gbps)
- Support DPCD **Rev.1.1**
- Support HDCP **1.3** with HDCP key embedded
- Support Spread Spectrum Clocking up to **0.5%** down-spread to reduce EMI
- Support Source Connection Detection through AUX channel DC levels
- Support up to **WQXGA(2560X1600)** VESA display format
- Support Digital Video Output in 18/24/30/36(deep color) bits format with separate Sync control
- Support Pixel component format with RGB; YCbCr 422; YCbCr 444
- Support Bit depth per color with 6/8/10/12 bits
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.
- Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
- Dithering for conversion from 12-bit component to 10-bit/8-bit
- S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio up to 192kHz frame rate
- Support 8-channel, uncompressed LPCM I2S audio with sample rates of 32~192 kHz and sample sizes of 16~24 bits
- Automatic Audio Error detection with soft mute function, preventing annoying harsh output sound due to audio error or hot-unplug

- Automatic loss of signal detection for Link management
- Intelligent, programmable power management
- 144-pin LQFP (20mm x 20mm) package

Pin Diagram



IT6506 provides internal register accessed via PCSCL (pin 71) and PCSDA (pin 70) with slave address 0xB0 where PCADR (pin68) is low, or 0xB2 where PCADR (pin68) is high under 100KHz speed.

The terms listed in the below table are using in future chapters:

Term	Description	Example
RegXX	Where XX is a hexadecimal number, to indicate the internal register accessed with subaddress XX of I^2C, and in bank 0.	Reg05 – access with I^2C slave address 0xB0/0xB2, sub-address 0x05.

Reg1XX	Where XX is a hexadecimal number, to indicate the internal register accessed with subaddress XX of I^2C, and in bank 1.	Reg1C0 – access with I^2C slave address 0xB0/0xB2, sub-address 0xC0.
Reg2XX	Where XX is a hexadecimal number, to indicate the internal register accessed with subaddress XX of I^2C, and in bank 2.	

The register 0x00~0x0F are common for all banks, and the bank switching using as following:

bank 0 – reg05[3][0] = '0' '0'

bank 1 – reg05[3][0] = '0' '1'

bank 2 – reg05[3][0] = '1' '0'

Chap 2 IT6506 Initial

IT6506 initial can be separated into two parts. The first part is to reset the physical layer of IT6506. The second part is to reset the logical part of IT6506.

Initial Register Setting

The following table is the setting sequence for each step. The Bit Mask means the bit to update on each step, and the Bit Value means the updating part of each step.

Reg	Bit Mask	Bit Value
0xEA	0xFF	0xFF
0xEA	0xFF	0x10
0xEB	0xFE	0xFE
0x1B3	0xFE	0xFE
0x1B3	0xFE	0x00
0x1B2	0xFF	4
0x1B2	0x05	1
0x1B5	0xFF	0x14
0x1B7	0xFF	0x33
0x1B8	0xFF	0x03
0x1CD	0xFF	0x80
0x1D2	0xFF	0x88
0x1D3	0xFF	0x69
0xEA	0x05	0x05
0xEA	0x05	0x04
0xEE	0x01	0x01
0x21	0xFF	0x0A
0x22	0xFF	0x64
0x2F	0xFF	0x7B
0xFD	0x05	4
0x31	0x40	0x40
0x32	0xFF	0xFF
0xB2	0x41	1
0xB7	0xFF	0x10
0xB8	0xFF	0x08
0xB9	0xFF	0x10
0xBA	0xFF	0x08
0xBB	0xFF	0x30
0xBC	0xFF	0x60
0xBD	0xF0	0x00
0xC0	0xFF	0x00
0xC1	0xBF	0xBF
0xC2	0xFF	0x8C
0xC3	0xFF	0x7A
0xCC	0xFF	0xC5
0xCD	0xFF	0xA8
0xE3	0x80	0x80
0xEB	0x8F	0xF
0xEC	0x26	0x26
0xEF	0x24	0x24
0xF1	0x40	0x40
0xFC	0xFF	0x21
0xD2	0xFF	0xE0
0xF6	0xFF	0x4C
0x1A5	0xFF	0xC8
0x1A2	0x10	0x00
0x1B1	0x04	0x04
0x1B1	0x78	0x00
0x170	0x0C	0x04
0xE4	0xFF	0x00

0xE6	0xFF	0x00
0xE9	0xFF	0x00
0xE5	0xFF	0x07
0xE7	0xFF	0xFF
0xE8	0xFF	0xFF
0xC9	0x09	0x09
0xED	0xC0	0x80
0xEE	0x02	0x00
0xEE	0xFC	0xFC
0xC9	0x10	0x10
0xF7	0x01	0x00

Chap 3 Event of IT6506

The events of IT6506 will activate the bits in reg06, where each bit corresponded to a group of event shows in the table reg07~reg0C.

Reg	Name	Bit	Descrioption	Type
06	Reserved	7:6	----------	RO
	IntGroup5	5	Group Reg0Ch Int	RO
	IntGroup4	4	Group Reg0Bh Int	RO
	IntGroup3	3	Group Reg0Ah Int	RO
	IntGroup2	2	Group Reg09h Int	RO
	IntGroup1	1	Group Reg08h Int	RO
	IntGroup0	0	Group Reg07h Int	RO

The event of IT6506 shows on the register Reg07~Reg0C, as the following table, where write to one will clear the bits.

Reg	Name	Bit	Descrioption	Type
07	LSVBIDInt	7	VBID majority error interrupt	W1C
	LSNAudInt	6	NAud majority error interrupt	W1C
	LSMAudInt	5	Maud majority error interrupt	W1C
	LSMVidInt	4	Mvid majority error interrupt	W1C
	RegAFUflow	3	Audio fifo under flow	RO
	RegAFOflow	2	Audio fifo over flow	RO
	RegVFUflow	1	video fifo under flow	RO
	RegVFOflow	0	video fifo over flow	RO
08	LSAudMuteEnd	7	Audio mute end interrupt	W1C
	LSAudMuteStart	6	Audio mute start interrupt	W1C
	LSVidMuteEnd	5	Video mute end interrupt	W1C
	LSVidMuteStart	4	Video mute start interrupt	W1C
	AutoAudMute	3	Write 1 will gen REGHWMuteAACClr	W1C
	RefAuxURLen	2	AUX receive un-support length interrupt	W1C
	RefAuxURCmd	1	AUX receive un-support command interrupt	W1C
	RefAuxSynErr	0	AUX receive sync length error interrupt	W1C
09	LSNoSPDInfo	7	No SPD InfoFrame interrupt	W1C
	LSNoMpegInfo	6	No Mpeg InfoFrame interrupt	W1C
	LSNoAudInfo	5	No Audio InfoFrame interrupt	W1C
	LSNoAVIInfo	4	No AVI InfoFrame interrupt	W1C
	LSL3ECCInt	3	Lane 3 (2 nibble error) ECC interrupt	W1C
	LSL2ECCInt	2	Lane 2 (2 nibble error) ECC interrupt	W1C
	LSL1ECCInt	1	Lane 1 (2 nibble error) ECC interrupt	W1C
	LSL0ECCInt	0	Lane 0 (2 nibble error) ECC interrupt	W1C
0A	RefL3SymUnLkIRQ	7	Lane 3 Symbol lose lock interrupt	W1C
	RefL2SymUnLkIRQ	6	Lane 2 Symbol lose lock interrupt	W1C
	RefL1SymUnLkIRQ	5	Lane 1 Symbol lose lock interrupt	W1C
	RefL0SymUnLkIRQ	4	Lane 0 Symbol lose lock interrupt	W1C
	RefLnkTrnFalIRQ	3	Link Training fail interrupt	W1C
	RefSymUnAlgnIRQ	2	Symbol lose alignment interrupt	W1C
	RefLnkTrnDnIRQ	1	Link Training done interrupt	W1C
	RefLnkTrnStrIRQ	0	Link Training start interrupt	W1C
0B	RefAuthDnIRQ	7	Authentication done interrupt	W1C
	RefAuthStartIRQ	6	Authentication start interrupt	W1C
	RefLCFailIRQ	5	Link Integrity Check fail interrupt	W1C
	RefRiRdyIRQ	4	R0 ready interrupt	W1C
	RefAksvFailIRQ	3	Illegal Aksv interrrupt	W1C
	RefHPDRstNIRQ	2	HPD Reset interrupt	W1C
	RefD3EntryInt	1	DPCD 00600h[1:0] have been changed to 10 from other values	W1C
	RefD0EntryInt	0	DPCD 00600h[1:0] have been changed to 01 from other values	W1C
0C	Reserved	7	----------	RO

	LSNewGenPkt	6	New Mpeg InfoFrame interrupt	W1C
	LSNewSPDInfo	5	New SPD InfoFrame interrupt	W1C
	LSNewMpegInfo	4	New Mpeg InfoFrame interrupt	W1C
	LSNewAudInfo	3	New Audio InfoFrame interrupt	W1C
	LSNewAVIInfo	2	New AVI InfoFrame interrupt	W1C
	LSNewVidFormat	1	New Video format interrupt	W1C
	RefI2CHangInt	0	I2C may hanging (stay the same state too long)	W1C
0D	LSL32NibbleErr	7	Lane 3 ECC 2 nibble error	W1C
	LSL22NibbleErr	6	Lane 2 ECC 2 nibble error	W1C
	LSL12NibbleErr	5	Lane 1 ECC 2 nibble error	W1C
	LSL02NibbleErr	4	Lane 0 ECC 2 nibble error	W1C
	LSL31NibbleErr	3	Lane 3 ECC 1 nibble error	W1C
	LSL21NibbleErr	2	Lane 2 ECC 1 nibble error	W1C
	LSL11NibbleErr	1	Lane 1 ECC 1 nibble error	W1C
	LSL01NibbleErr	0	Lane 0 ECC 1 nibble error	W1C

Where interrupt mask is in RegE4~RegE9, and the bits are one-to-one mapping to reg07~reg0C:

Reg	Name	Bit	Description	Type	Default Value
E4	RegIntMask[7:0]	7:0	Interrupt Mask [7:0] For register 07 (one to one mapping)	R/W	11111111
E5	RegIntMask[15:8]	7:0	Interrupt Mask [15:8] For register 08	R/W	11111111
E6	RegIntMask[23:16]	7:0	Interrupt Mask [23:16] For Register 09	R/W	11111111
E7	RegIntMask[31:24]	7:0	Interrupt Mask [31:24] For Register 0A	R/W	11111111
E8	RegIntMask[39:32]	7:0	Interrupt Mask [39:32] For Register 0B	R/W	11111111
E9	RegIntMask[47]	7	Reserved For future use	R/W	1
	RegIntMask[46:40]	6:0	For Resister 0C[6:0]	R/W	1111111

Chap 4 Link Configuration

Hot Plug

IT6506 can determine the HPD to Tx side with regC9[4] = '1' for plugged and '0' for unplugged.

Trigger HPD interrupt with reg1F[6] to notify DP source device.

System status

The following register regC8 shows the system status of IT6506:

reg	name	bit	description	type
C8	Reserved	7:6	----------	
	RegLnkTrnFail	5	Link Training fail status	RO
	RegTxSense	4	Tx Sense status	RO
	RegTxPwrSense	3	Tx power is on	RO
	RegTxConnected	2	Tx is connected	RO
	RegLnkTrnDn	1	Link Training done status	RO
	RegLnkTrnBusy	0	Link Training busy status	RO

The system state transition can refer these bits to judge the status transition.

IT6506 Capacity Configuring

Set DP sink capability with the following table:

Feature	Reg Setting
Acceptable Maximum Lane Number	4 lanes – reg22[2:0] = '100' 2 lanes – reg22[2:0] = '010' 1 lane – reg22[2:0] = '001'
SSC	reg22[6] = '1' for enabling
Enhance Framing	reg22[5] = '1' for enabling

Detecting a Tx

regC8[4] = '1', means a DP 1.1a transmitter connected.

Training

When DisplayPort transmitter start link training, regC8[0] will be read back as '1'. If training done, regC8[1] = '1' until next training start or fail.

After training done, the video and audio can be measuring.

Train Fail

Detecting a training fail in regC8[4] = '1', the training fail.

Chap 5 Video Programming

If DP connection are built and trained, the video will be sent from DP source. Video and audio input status are present in reg11:

11	Reserved	7:6	----------	RO
	RegAudStable	5	Audio output stable	RO
	RegVidStable	4	video output stable	RO

Video Input Readback

And begin to program the video output and pass the video parameter defined in the following registers:

Input Video Pixel Clock is in reg11[3:0]|10[7:0]

10	RegPClkCnt[7:0]	7:0	PCLKCnt = the tick count of PCLK under 1024T of 27MHz reference clock. PCLK = 27MHz*1024/PCLKCnt	RO	
11	Reserved	7:6		RO	
	RegAudStable	5	Audio output stable	RO	
	RegVidStable	4	video output stable	RO	
	RegPClkCnt[11:8]	3:0		RO	

If RegPclkCnt = 186, PCLK = 27MHz * 1024/186 = 148.6MHz

Input Video status registers:

Reg	Name	bit	Description	Type
97	LSHTotal [7:0]	7:0	H total [7:0]	RO
98	LSHTotal [15:8]	7:0	H total [15:8]	RO
99	LSHStart[7:0]	7:0	H start [7:0] from Hsync start edge to H active start edge	RO
9A	LSHStart[15:8]	7:0	H start [15:8] from Hsync start edge to H active start edge	RO
9B	LSHWidth[7:0]	7:0	Main stream attribute data - H active width [7:0]	RO
9C	LSHWidth[15:8]	7:0	Main stream attribute data -H active width [15:8]	RO
9D	LSVTotal[7:0]	7:0	Main stream attribute data -V total [7:0]	RO
9E	LSVTotal[15:8]	7:0	Main stream attribute data -V total [15:8]	RO
9F	LSVStart[7:0]	7:0	Main stream attribute data -V start [7:0] from Vsync start edge to V active start edge	RO
A0	LSVStart[15:8]	7:0	Main stream attribute data -V start [15:8] from Vsync start edge to V active start edge	RO
A1	LSVHeight[7:0]	7:0	Main stream attribute data -V active height [7:0]	RO
A2	LSVHeight[15:8]	7:0	Main stream attribute data -V active height [15:8]	RO
A3	LSHSyncWidth[7:0]	7:0	Main stream attribute data -H Sync Width [7:0]	RO
A4	LSHSyncPolarity	7	Main stream attribute data -H Sync polarity	RO
	LSHSyncWidth[14:8]	6:0	Main stream attribute data -H Sync Width[14:8]	RO
A5	LSVSyncWidth	7:0	Main stream attribute data -V Sync Width [7:0]	RO
A6	LSVSyncPolarity	7	Main stream attribute data -VSync polarity	RO
	LSVSyncWidth	6:0	Main stream attribute data -V Sync Width[7:0]	RO
A7	LSVdBPC	7:5	Main stream attribute data -Bit depth per color / component 000 = 6 bits 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 16 bits 101, 110, 111 = Reserved	RO
	LSVdYUVColor	4	Main stream attribute data -YCbCr Colorietry 0: ITU-R BT601-5 1: ITU-R BT709-5	RO

	LSVdRange	3	Main stream attribute data -Dynamic range 0: VESA range (from 0 to the maximum) 1: CEA range	RO
	LSVdPxlFormat	2:1	Main stream attribute data -Component format 00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 11: Reserved	RO
	LSCLKSync	0	Main stream attribute data -Synchronous clock 0: Link clock and stream clock asynchronous 1: Link clock and stream clock synchronous	RO
A8	Reserved	7:3	----------	RO
	LSStereoVdAttr	2:1	Main stream attribute data -Stereo video attribute 00: No stereo video transported 01: for progressive vide, the next frame is RIGHT eye, for interlaced video, TOP field is RIGHT eye and BOTTOM field is LEFT eye 10: reserved and must not be used 11: for progressive video, the next frame is LEFT eye, for interlaced video, TOP field is LEFT eye and BOTTOM field is RIGHT eye	RO
	LSVdIFrameEven	0	Main stream attribute data -Interlaced vertical total even 0: number of lines per interlaced frame (consisting of two fields) is an odd number 1: number of lines per interlaced frame (consisting of two fields) is an even number	RO

Video Output Programming

Video output path control registers are listed in the following table:

Reg	Name	bit	Description	Type	Default Value
170	Reg_LMSwap	7	1: swap output direction(MSB/LSB)	R/W	0
	Reg_O16Bit	6	'1' : YCbCr422 output only 16bit width '0': YCbCr422 output is 24/20 bit width.	R/W	0
	Reg_OUTBit	5:4	00: output 8 bits per color channel 01:output 10 bits per color channel 10:output 12 bits per color channel 11: reserved	R/W	00
	Reg_ColorDepth	3:2	00: output 8 bits 444 format 01: output 10 bits 444 format 10: output 12 bits 444 format	R/W	01
	Reg_PCLKDiv2	1	'1': output half PCLK	R/W	0
	Reg_ChgSyncPol	0	'1': output H/V sync indicated by reg171[2]/reg171[3] '0': keep the original sync polarity.	R/W	0
171	Reg_PGEn	7	reserved	R/W	0
	Reg_DNFreeGo	6	'1': Dither free go.	R/W	0
	Reg_EnUdFilt	5	'1': Enable 444 ↔ 422 up/down filter	R/W	0
	Reg_EnDither	4	'1': Enable Dither	R/W	0
	Reg_VSyncPol	3	'1': Set V sync polarity as positive while reg170[0] as '1' '0': Set V sync polarity as negative while reg170[0] as '1'	R/W	0
	Reg_HSyncPol	2	'1': Set H sync polarity as positive while reg170[0] as '1' '0': Set YH sync polarity as negative while reg170[0] as '1'	R/W	0
	Reg_ChSwap	1	'1': Swap output R/B(Cr/Cb) channel	R/W	0
	Reg_RBSwap	0	'1': Swap input R/B(Cr/Cb) channel	R/W	0

To determine the output color mode, the setting are listed as following:

Output RGB444 video

The output value should be:

		bit	Value
170	Reg_LMSwap	7	0
	Reg_O16Bit	6	0
	Reg_OUTBit	5:4	
	Reg_ColorDepth	3:2	
	Reg_PCLKDiv2	1	0
	Reg_ChgSyncPol	0	0
171	Reg_PGEn	7	0
	Reg_DNFreeGo	6	x
	Reg_EnUdFilt	5	x
	Reg_EnDither	4	x
	Reg_VSyncPol	3	x
	Reg_HSyncPol	2	x
	Reg_ChSwap	1	x
	Reg_RBSwap	0	x
176	Reg_SyncEmb	3	0
18F	Reg_OutDDR	7	0
	Reg_2x656Clk	6	0
	Reg_656FFRst	5	0
	Reg_EnAVMuteRst	4	0
	Reg_CSCSel	3:2	00 / 02
	Reg_OutColMod	1:0	00

Output YCbCr444 video

The output value should be:

		bit	Value
170	Reg_LMSwap	7	0
	Reg_O16Bit	6	0
	Reg_OUTBit	5:4	
	Reg_ColorDepth	3:2	
	Reg_PCLKDiv2	1	0
	Reg_ChgSyncPol	0	0
176	Reg_SyncEmb	3	0
171	Reg_PGEn	7	0
	Reg_DNFreeGo	6	x
	Reg_EnUdFilt	5	x
	Reg_EnDither	4	x
	Reg_VSyncPol	3	x
	Reg_HSyncPol	2	x
	Reg_ChSwap	1	x
	Reg_RBSwap	0	x
18F	Reg_OutDDR	7	0
	Reg_2x656Clk	6	0
	Reg_656FFRst	5	0
	Reg_EnAVMuteRst	4	0
	Reg_CSCSel	3:2	00 / 03
	Reg_OutColMod	1:0	10

Output YCbCr422 video sync seperated

The output value should be:

		bit	Value
170	Reg_LMSwap	7	0

	Reg_O16Bit	6	x
	Reg_OUTBit	5:4	00
	Reg_ColorDepth	3:2	00
	Reg_PCLKDiv2	1	0
	Reg_ChgSyncPol	0	0
176	Reg_SyncEmb	3	0
171	Reg_PGEn	7	0
	Reg_DNFreeGo	6	x
	Reg_EnUdFilt	5	x
	Reg_EnDither	4	x
	Reg_VSyncPol	3	x
	Reg_HSyncPol	2	x
	Reg_ChSwap	1	x
	Reg_RBSwap	0	x
18F	Reg_OutDDR	7	0
	Reg_2x656Clk	6	0
	Reg_656FFRst	5	0
	Reg_EnAVMuteRst	4	0
	Reg_CSCSel	3:2	00 / 03
	Reg_OutColMod	1:0	01

Output YCbCr422 video sync embedded

The output value should be:

		bit	Value
170	Reg_LMSwap	7	0
	Reg_O16Bit	6	0
	Reg_OUTBit	5:4	00
	Reg_ColorDepth	3:2	00
	Reg_PCLKDiv2	1	0
	Reg_ChgSyncPol	0	0
176	Reg_SyncEmb	3	1
171	Reg_PGEn	7	0
	Reg_DNFreeGo	6	x
	Reg_EnUdFilt	5	x
	Reg_EnDither	4	x
	Reg_VSyncPol	3	x
	Reg_HSyncPol	2	x
	Reg_ChSwap	1	x
	Reg_RBSwap	0	x
18F	Reg_OutDDR	7	0
	Reg_2x656Clk	6	0
	Reg_656FFRst	5	0
	Reg_EnAVMuteRst	4	0
	Reg_CSCSel	3:2	00 / 02
	Reg_OutColMod	1:0	00

Output YCbCr422 video sync embedded CCIR656

The output value should be:

		bit	Value
170	Reg_LMSwap	7	0
	Reg_O16Bit	6	0
	Reg_OUTBit	5:4	00
	Reg_ColorDepth	3:2	00
	Reg_PCLKDiv2	1	0
	Reg_ChgSyncPol	0	0
171	Reg_PGEn	7	0
	Reg_DNFreeGo	6	x
	Reg_EnUdFilt	5	x

	Reg_EnDither	4	x
	Reg_VSyncPol	3	x
	Reg_HSyncPol	2	x
	Reg_ChSwap	1	x
	Reg_RBSwap	0	x
176	Reg_SyncEmb	3	1
18F	Reg_OutDDR	7	0
	Reg_2x656Clk	6	1
	Reg_656FFRst	5	0
	Reg_EnAVMuteRst	4	0
	Reg_CSCSel	3:2	00 / 02
	Reg_OutColMod	1:0	00

Color Converting

If the input color and output color need a color space convert, the convert matrix are defined in the following registers:

Reg	Name	bit	description	Type	default
173	Reg_YOffSet	7:0		R/W	00000000
174	Reg_COffSet	7:0		R/W	00000000
175	Reg_RGBOffSet	7:0		R/W	00000000
190	Reg_Matrix11V[7:0]	7:0	CSC matrix 11 low byte	R/W	10110010
191	Reserved	7:6	----------	RO	
	Reg_Matrix11V[13:8]	5:0	CSC matrix 11 high bits	R/W	000100
192	Reg_Matrix12V[7:0]	7:0	CSC matrix 12 low byte	R/W	01100100
193	Reserved	7:6	----------	RO	
	Reg_Matrix12V[13:8]	5:0	CSC matrix 12 high bits	R/W	000010
194	Reg_Matrix13V[7:0]	7:0	CSC matrix 13 low byte	R/W	11101001
195	Reserved	7:6	----------	RO	
	Reg_Matrix13V[13:8]	5:0	CSC matrix 13 high bits	R/W	000000
196	Reg_Matrix21V[7:0]	7:0	CSC matrix 21 low byte	R/W	10010011
197	Reserved	7:6	----------	RO	
	Reg_Matrix21V[13:8]	5:0	CSC matrix 21 high bits	R/W	011100
198	Reg_Matrix22V[7:0]	7:0	CSC matrix 22 low byte	R/W	00010110
199	Reserved	7:6	----------	RO	
	Reg_Matrix22V[13:8]	5:0	CSC matrix 22 high bits	R/W	000100
19A	Reg_Matrix23V[7:0]	7:0	CSC matrix 23 low byte	R/W	01010110
19B	Reserved	7:6	----------	RO	
	Reg_Matrix23V[13:8]	5:0	CSC matrix 23 high bits	R/W	011111
19C	Reg_Matrix31V[7:0]	7:0	CSC matrix 31 low byte	R/W	01001001
19D	Reserved	7:6	----------	RO	
	Reg_Matrix31V[13:8]	5:0	CSC matrix 31 high bits	R/W	011101
19E	Reg_Matrix32V[7:0]	7:0	CSC matrix 32 low byte	R/W	10011111
19F	Reserved	7:6	----------	RO	
	Reg_Matrix32V[13:8]	5:0	CSC matrix 32 high bits	R/W	011110
1A0	Reg_Matrix33V[7:0]	7:0	CSC matrix 33 low byte	R/W	00010110
1A1	Reserved	7:6	----------	RO	
	Reg_Matrix33V[13:8]	5:0	CSC matrix 33 high bits	R/W	000100

To setting the matrix, depends the input color and output color mapping:

Color space converting table		RGB to YUV				YUV to RGB			
		RGB to YUV 601		RGB to YUV 709		YUV to RGB 601		YUV to RGB 709	
	reg	16~ 235	0 ~ 255	16~ 235	0 ~ 255	16~ 235	0 ~ 255	16~ 235	0 ~ 255
Reg_CSCSel[1:0]	18F[3:2]	10	10	10	10	11	11	11	11
Reg_YoffSet[7:0]	173	0x00	0x10	0x00	0x10	0x00	0x10	0x00	0x10
Reg_CoffSet[7:0]	174	0x80	0x80	0x80	0x80	0x80	0x80	0x80	0x80
Reg_RGBOffSet[7:0]	175	0x00	0x10	0x00	0x10	0x00	0x10	0x00	0x10
Reg_Matrix11V[13:0]	190	0xB2	0x09	0xB8	0xE5	0x00	0x4F	0x00	0x4F
	191	0x04	0x04	0x05	0x04	0x08	0x09	0x08	0x09

Reg_Matrix12V[13:0]	192	0x64	0x0E	0xB4	0x78	0x6A	0x81	0x53	0xBA
	193	0x02	0x02	0x01	0x01	0x3A	0x39	0x3C	0x3B
Reg_Matrix13V[13:0]	194	0xE9	0xC8	0x93	0x81	0x4F	0xDF	0x89	0x4B
	195	0x00	0x00	0x00	0x00	0x3D	0x3C	0x3E	0x3E
Reg_Matrix21V[13:0]	196	0x93	0x0E	0x49	0xCE	0x00	0x4F	0x00	0x4F
	197	0x3C	0x3D	0x3C	0x3C	0x08	0x09	0x08	0x09
Reg_Matrix22V[13:0]	198	0x18	0x84	0x18	0x84	0xF7	0xC2	0x51	0x56
	199	0x04	0x03	0x04	0x03	0x0A	0x0C	0x0C	0x0E
Reg_Matrix23V[13:0]	19A	0x56	0x6E	0x9F	0xAE	0x00	0x00	0x00	0x00
	19B	0x3F	0x3F	0x3F	0x3F	0x00	0x00	0x00	0x00
Reg_Matrix31V[13:0]	19C	0x49	0xAC	0xD9	0x49	0x00	0x4F	0x00	0x4F
	19D	0x3D	0x3D	0x3C	0x3D	0x08	0x09	0x08	0x09
Reg_Matrix32V[13:0]	19E	0x9F	0xD0	0x10	0x33	0x00	0x00	0x00	0x00
	19F	0x3E	0x3E	0x3F	0x3F	0x00	0x00	0x00	0x00
Reg_Matrix33V[13:0]	1A0	0x18	0x84	0x18	0x84	0xDB	0x1E	0x87	0xE7
	1A1	0x04	0x03	0x04	0x03	0x0D	0x10	0x0E	0x10

Enable Video Output

Set Reg35[3] as zero to enable video output.

To enable video IO, regEB[5:4] = ‘00’

To enable video data output, in single pixel mode, regEE[7:2] = ‘111000’; if under dual pixel mode, regEE[7:2] = ‘000000’ .

Chap 6 Audio Programming

RegEA[2] = '0', the audio program is available.

The audio related registers are listed as following table:

Audio Control Register

reg	Name	bit	description	type	Default
88	LSAudStrID	7:0	Audio stream packet ID	RO	
89	LSAudStrCType	6:3	Audio stream coding type	RO	
	LSAudStrChCnt	2:0	Audio stream channel count	RO	
F6	RegWs_sel	7	I2S word select switch 0: left -> right, 1:right->left	R/W	0
	RegACINC	6		R/W	0
	RegMCLKSel	5:4		R/W	01
	RegARDec	3:2		R/W	00
	RegAPLLGain	1:0		R/W	01
F7	RegI2s_mode	7:6	I2S mapping mode select 00:i2s, 01:right, 10:left, 11:raw 60958	R/W	00
	RegAudVolCtrl	5:4	Audio volume control	R/W	00
	RegHWAudMuteClrMode	3	Audio hardware mute clear enable	R/W	0
	RegBiphasemode	2	SPDIF output enable	R/W	0
	RegHWMuteClr	1	Audio hardware mute clear	R/W	0
	RegHWMuteEn	0	Audio hardware mute enable	R/W	0
F8	RegI2S_CH3SEL	7:6	I2S channel 3 output source select	R/W	11
	RegI2S_CH2SEL	5:4	I2S channel 2 output source select	R/W	10
	RegI2S_CH1SEL	3:2	I2S channel 1 output source select	R/W	01
	RegI2S_CH0SEL	1:0	I2S channel 0 output source select	R/W	00
F9	RegHWMuteRate[7:0]	7:0	Audio hardware mute rate low byte	R/W	00100000
FA	RegI2s_width	7:3	I2S word length select	R/W	11000
	RegHWMuteRate[10:8]	2:0	Audio hardware mute rate high bits	R/W	000
FB	Reserved	7:6	----------	RO	
	RegFSdec	3:0	Sample frequency indicated in *IEC60958-3 p11 bit 24~27*. Sample frequency of software indicated 27..24 -------- 0000 44.1 KHz 1000 88.2 KHz 1100 176.4 KHz 0110 24 Khz 0010 48Khz 1010 96Khz 1110 192KHz 0011 32KHz 0000 sampling frequency not indicated.	RO	

The output value can be decided in the initial stage, and only enable audio output while the audio stable in Reg35[1].

Audio Input Information

Audio is stable when reg10[5] = '1'. If no audio stable, and no overflow/underflow interrupt arriving, there is no audio.

If audio input change or invalid, the audio FIFO overflow/underflow interrupt responds in reg07[3][2]. When audio change and invalid, reset audio (regEA[2] = '1') and wait for audio input stable again.

Audio channel number is presented on reg89[2:0], and sample frequency is presented on regFB[3:0].

Configure Audio Output

When audio input is available, following the steps described below to configure audio output.

1. regEA[2] = '0'.
2. reg1B1[2] = '0'
3. reg1B3[2] = '1', regEA[2] = '1'
4. reg1B3[2] = '0', regEA[2] = '0'
5. If mini mode, set regF5[7] = '1', otherwise, set is as '0'.
6. Enable audio output from IT6505:
   - If require SPDIF output, set regEB[3] = '0'.
   - If require I2S for 5~8 channel audio, set regEB[2][1] = '0' '0'
   - If only require I2S audio with 1~4 channel, set regEB[2][1] = '1' '0'

Audio Error

If audio input have error, audio will be automatic mute by IT6506. The interrupt of audio overflow/underflow will be activated. When audio error, reset the audio circuit with regEA[2] = '1', then reprogram the audio with previous sequence.

DPCD Offset	Name	Count	Reg map	Reg Mod	Funcgtion
68000	BKSV	5	130		HDCP registers are located in DPCD address 0x68000~0x6803A, which are mapping to IT6504 bank 1 register 30~6A. Those registers are read only, and the register should update by other registers.
68005	R0′	2	135		
68007	AKSV	5	137		
6800C	An	8	13C		
68014	V′ H1	4	144	224 225 226 227	The V' calculation should do the SHA-1 calculation via software. No hardware way to calculate. The calculation of V' (reg224~reg237) need KSVList (reg15C~reg16A),
68018	V′ H2	4	148	228 229 22A 22B	
6801C	V′ H3	4	14C	22C 22D 22E 22F	
68020	V′ H4	4	150	230 231 232 233	
68024	V′ H5	4	154	234 235 236 237	
68028	BCaps	1	158		bit 1 – REPEATER RegCF[2] RegSetRepeater = this bit bit 0 – HDCP_CAPABLE RegB2[0] RegCPDesired
68029	BStatus	1	159		bit 2 – link ingtegrity_fail – loss of cipher synchronizationi. bit 1 – R0 Available bit 0 – Ready – HDCP repeater KSV FIFO ready. Bstatus[2], LINK_INTEGRITY_FAILURE, is indicated by the HW. Bstatus[1], R0'_AVALILABLE, is indicated by the HW. Bstatus[0], READY, is programed by RegCF[1], RegSetVReady.
6802A	BInfo	1	15A	238 239	bit 11 – MAX_CASCADE_EXCEEDED bit [10:8] – DEPTH bit [7] – MAX_DEV_EXCEEDED bit[6:0] – Downstream counter
6802C	KSV FIFO	15	15C		

RegCF[0] – CPReady set.

RegCF[1] – write ‘1’ to trigger 68029[0] as ‘1’, and need to clear immediatly.

Reg	Name	Type	Description	
1E3	invM0[7:0]	R/O	inverse of M0	
1E4	invM0[15:8]	R/O		
1E5	invM0[23:16]	R/O		
1E6	invM0[31:24]	R/O		
1E7	invM0[39:32]	R/O		
1E8	invM0[47:40]	R/O		
1E9	invM0[55:48]	R/O		
1EA	invM0[63:56]	R/O		
210~214	KSV0	R/W		
215~219	KSV1	R/W		
21A~21E	KSV2	R/W		
21F~223	KSV3	R/W		
224~237	VH	R/W		

238	bInfo[7:0]	R/W		
239	bInfo[15:0]	R/W		

Chap 9 Registers

W1C：Write 1 Clear
R1C：Read Clear
RO：Read Only
R/W：Read and Write
Note: There are two register banks in IT6506 register table, for Bank1 registers selection, the reg0x05[0]=0. For Bank2 registers selection, the reg0x05[0]=1.

Bank 0 : reg05[3] = '0', reg05[0] = '0'

Reg	Register Name	Bit	Definition	Type	Default Value
00	DevNum_L	7:0	Device number low byte	RO	06
01	DevNum_H	7:0	Device number high byte	RO	05
02	RevNum	7:0	Revision number	RO	B0
05	Reserved	7:4		RO	
	RegBankSel[1]	3	Select the register bank bit[1]	R/W	0
	RegLCForce	2	Programming the DPCD 100 – 107 value through uP 1: enable force linktrain configuration set 0: disable	R/W	
	RegEDIDWP	1		R/W	1
	RegBankSel	0	Select the register bank bit[0] 00: select bank 0 01: select bank 1 10: select bank 2	R/W	0
06	Reserved	7:6		RO	
	IntGroup5	5	Group Reg0Ch Int	RO	
	IntGroup4	4	Group Reg0Bh Int	RO	
	IntGroup3	3	Group Reg0Ah Int	RO	
	IntGroup2	2	Group Reg09h Int	RO	
	IntGroup1	1	Group Reg08h Int	RO	
	IntGroup0	0	Group Reg07h Int	RO	
07	LSVBIDInt	7	VBID majority error interrupt	W1C	
	LSNAudInt	6	NAud majority error interrupt	W1C	
	LSMAudInt	5	Maud majority error interrupt	W1C	
	LSMVidInt	4	Mvid majority error interrupt	W1C	
	RegAFUflow	3	Audio fifo under flow	RO	
	RegAFOflow	2	Audio fifo over flow	RO	
	RegVFUflow	1	video fifo under flow	RO	
	RegVFOflow	0	video fifo over flow	RO	
08	LSAudMuteEnd	7	Audio mute end interrupt	W1C	
	LSAudMuteStart	6	Audio mute start interrupt	W1C	
	LSVidMuteEnd	5	Video mute end interrupt	W1C	
	LSVidMuteStart	4	Video mute start interrupt	W1C	
	AutoAudMute	3	Write 1 will gen REGHWMuteAACClr	W1C	
	RefAuxURLen	2	AUX receive un-support length interrupt	W1C	
	RefAuxURCmd	1	AUX receive un-support command interrupt	W1C	
	RefAuxSynErr	0	AUX receive sync length error interrupt	W1C	
09	LSNoSPDInfo	7	No SPD InfoFrame interrupt	W1C	
	LSNoMpegInfo	6	No Mpeg InfoFrame interrupt	W1C	
	LSNoAudInfo	5	No Audio InfoFrame interrupt	W1C	
	LSNoAVIInfo	4	No AVI InfoFrame interrupt	W1C	
	LSL3ECCInt	3	Lane 3 (2 nibble error) ECC interrupt	W1C	
	LSL2ECCInt	2	Lane 2 (2 nibble error) ECC interrupt	W1C	
	LSL1ECCInt	1	Lane 1 (2 nibble error) ECC interrupt	W1C	
	LSL0ECCInt	0	Lane 0 (2 nibble error) ECC interrupt	W1C	
0A	RefL3SymUnLkIRQ	7	Lane 3 Symbol lose lock interrupt	W1C	

	RefL2SymUnLkIRQ	6	Lane 2 Symbol lose lock interrupt	W1C	
	RefL1SymUnLkIRQ	5	Lane 1 Symbol lose lock interrupt	W1C	
	RefL0SymUnLkIRQ	4	Lane 0 Symbol lose lock interrupt	W1C	
	RefLnkTrnFalIRQ	3	Link Training fail interrupt	W1C	
	RefSymUnAlgnIRQ	2	Symbol lose alignment interrupt	W1C	
	RefLnkTrnDnIRQ	1	Link Training done interrupt	W1C	
	RefLnkTrnStrIRQ	0	Link Training start interrupt	W1C	
0B	RefAuthDnIRQ	7	Authentication done interrupt	W1C	
	RefAuthStartIRQ	6	Authentication start interrupt	W1C	
	RefLCFailIRQ	5	Link Integrity Check fail interrupt	W1C	
	RefRiRdyIRQ	4	R0 ready interrupt	W1C	
	RefAksvFailIRQ	3	Illegal Aksv interrrupt	W1C	
	RefHPDRstNIRQ	2	HPD Reset interrupt	W1C	
	RefD3EntryInt	1	DPCD 00600h[1:0] have been changed to 10 from other values	W1C	
	RefD0EntryInt	0	DPCD 00600h[1:0] have been changed to 01 from other values	W1C	
0C	Reserved	7		RO	
	RefI2CHangInt	6	I2C may hanging (stay the same state too long)	W1C	
	LSNewVidFormat	5	New Video format interrupt	W1C	
	LSNewGenPkt	4	New Mpeg InfoFrame interrupt	W1C	
	LSNewSPDInfo	3	New SPD InfoFrame interrupt	W1C	
	LSNewMpegInfo	2	New Mpeg InfoFrame interrupt	W1C	
	LSNewAudInfo	1	New Audio InfoFrame interrupt	W1C	
	LSNewAVIInfo	0	New AVI InfoFrame interrupt	W1C	
0D	LSL32NibbleErr	7	Lane 3 ECC 2 nibble error	W1C	
	LSL22NibbleErr	6	Lane 2 ECC 2 nibble error	W1C	
	LSL12NibbleErr	5	Lane 1 ECC 2 nibble error	W1C	
	LSL02NibbleErr	4	Lane 0 ECC 2 nibble error	W1C	
	LSL31NibbleErr	3	Lane 3 ECC 1 nibble error	W1C	
	LSL21NibbleErr	2	Lane 2 ECC 1 nibble error	W1C	
	LSL11NibbleErr	1	Lane 1 ECC 1 nibble error	W1C	
	LSL01NibbleErr	0	Lane 0 ECC 1 nibble error	W1C	
0E	Reserved	7:6		RO	
	RegDEless	5		RO	
	RegDEover	4		RO	
	LSVBIDErr	3	VBID mahority error	W1C	
	LSNaudErr	2	Naud majority error	W1C	
	LSMaudErr	1	Maud majority error	W1C	
	LSMvidErr	0	Mvid majority error	W1C	
10	RegPClkCnt[7:0]	7:0	PCLKCnt = the tick count of PCLK under 1024T of 27MHz reference clock. PCLK = 27MHz*1024/PCLKCnt	RO	
11	Reserved	7:6		RO	
	RegAudStable	5	Audio output stable	RO	
	RegVidStable	4	video output stable	RO	
	RegPClkCnt[11:8]	3:0		RO	
1F	Reserved	7		RO	
	RefHPDIRQTrg	6	Trigger HPD interrrupt	W1P	
	RefDDCTrg	5	Trigger EMemory DDC accessing	W1P	
	RefAbortDDCTrg	4	Trigger EMemory abort DDC accessing	W1P	
	RefRdBksvTrg	3	Trigger Bksv reading	W1P	
	RefSinkSpecIRQ	2	Trigger the Sink_Specific_IRQ in DPCD (map to DPCD 201h[6])	W1P	
	RefAutoTestReq	1	Trigger the Automated_test_request in DPCD (map to DPCD 201h[1])	W1P	
	RefRmtCtlCmdPd	0	Trigger the remote_ctrl_cmd_pending in DPCD (map to DPCD 201h[0])	W1P	
20	RegDPCDRev	7:0	DPCD revision number (setting value for DPCD 000h)	R/W	00010001
21	RegMaxLinkRate	7:0	Maximum link rate of main link lanes (setting value for DPCD 001h)	R/W	00001010

22	RegNoAuxHSLT	7	0: Requires AUX CH handshake to sync. 1: Does not require AUX CH handshake to sync. (setting value for DPCD 003h[6])	R/W	0
	RegMaxDwnSpread	6	0: No down spread 1: 0.5% down spread (setting value for DPCD 003h[0])	R/W	1
	RegEnhFrameCap	5	0: Enhanced framing symbol sequence disabled. 1: Enhanced framing symbol sequence enabled. (setting value for DPCD 002h[7])	R/W	1
	RegMaxLaneCnt	4:0	The maximum number of lanes that sink device can support. (setting value for DPCD 002h[4:0])	R/W	00100
23	Reserved	7	----------	RO	
	RegOUISupport	6	0: OUI not supported 1: OUI supported	R/W	0
	Reg8B10BSupport	5	This bit set to 1 when DP receiver support the main link channel coding specification as specified in ANSI X3.230-1994, clause 11	R/W	1
	RegFmtConv	4	0: this branch device does not have a format conversion block 1: this downstream port has a format conversion block	R/W	0
	RegDSPortType	3:2	Indicates the downstream port type of port 0 00: Display Port 01: Analog VGA or analog video over DVI-I 10: DVI or HDMI 11: Others	R/W	0
	RegDSPortPret	1	Set to 1 when this device has downstream port	R/W	00
	RegNORP	0	Number of receiver ports	R/W	1
24	Reg1ATPrecPort	7	0: port 1 is used for main isochronous stream 1: port 1 is used for secondary isochronous stream of main stream received in the preceding port	R/W	0
	Reg1LEDIDPret	6	0: receiver port 1 has no local EDID 1: receiver port 1 has a local EDID	R/W	0
	Reg0ATPrecPort	5	0: port 0 is used for main isochronous stream 1: port 0 is used for secondary isochronous stream of main stream received in the preceding port	R/W	0
	Reg0LEDIDPret	4	0: receiver port 0 has no local EDID 1: receiver port 0 has a local EDID	R/W	1
	RegDSPortCnt	3:0	The number of downstream ports	R/W	0000
25	Reg0BufSize	7:0	Port 0's buffer size = (value+1) * 32 Bytes/lane	R/W	00000000
26	Reg1BufSize	7:0	Port 1's buffer size = (value+1) * 32 Bytes/lane	R/W	00000000
27	Reserved	7:4	----------	RO	
	RegDSPort0HPD	3	0: Downstream port is not HPD aware 1: Downstream port is HPD aware	R/W	0
	RegDSPort0Type	2:0	000: DisplayPort 001: Analog VGA 010: DVI 011: HDMI 100: others without EDID support 101~111 : Reserved	R/W	000
2B	Reserved	7	----------	RO	
	RegDSPortStChg	6	Set to 1 when any of the downstream ports has changed status	R/W	0
	RegSinkCnt	5:0	Total number of the sink devices within this device and those conneted to the downstream ports of this device	R/W	000000
2C	RegSinkOUI[7:0]	7:0	SINK_IEEE_OUI 7:0	R/W	00000000
2D	RegSinkOUI[15:8]	7:0	SINK_IEEE_OUI 15:8	R/W	00000000
2E	RegSinkOUI[23:16]	7:0	SINK_IEEE_OUI 23:16	R/W	00000000
2F	RegI2CMasterSel	7	0: I2C request feed from Aux Channel 1: I2C request feed from uP	R/W	0
	RegDebugMode	6:5	00: normal mode 11: simulation only mode	R/W	00
	Reg1usCntNo	4:0	Counter value for 1us	R/W	11011
30	RegBusHoldT	7:0	I2C Bus Hold Timer	R/W	00001000

31	RegRdStretch	7	1: Stretch I2C clock after mot=0 rd	R/W	0
	RegMonTxSense	6	0: Not monitor TxSense signal 1: Monitor TxSence signal	R/W	1
	RegRdRpyLenSel	5	0: read replay length equal to ready data length in FIFO 1: read replay length equal to Tx request length	R/W	1
	RegWrRpyLenSel	4	0: write replay length only include the length between two requests. 1: write replay length include the total bytes have been written from the write request start	R/W	1
	RegStrClrEn	3	0: internal stretch signal cleared when new request coming. 1: internal stretch signal not cleared when new request coming.	R/W	1
	RegHdrRpySel	2	0: ACK header when receive header and the request is not address only request. 1: Not ACK header when receive header and the request is not address only request.	R/W	1
	RegI2CAbort	1	I2C Abort request by uP	R/W	0
	RegI2CFifoClr	0	I2C FIFO Clear	R/W	0
32	RegI2CTOutSel	7:0	I2C TimeOut counter value	R/W	01000000
33	Reserved	7	----------	RO	
	Ref_BusHang	6	I2C bus hang	RO	
	Ref_Stus_ArbLose	5	I2C bus arbitration lose	RO	
	Ref_Stus_WaitBus	4	I2C wait bus	RO	
	Ref_Stus_NoACK	3	I2C no ack	RO	
	Ref_Stus_Done	2	I2C request done	RO	
	Ref_Active	1	I2C bus actived	RO	
	Ref_WaitBus	0	I2C in wait bus state	RO	
34	RegI2CEnRpStr	7	0: disable I2C repeat start 1: enable I2C repeat start	R/W	1
	RegAUXINSel	6	0: delay auxin From auxrxctrl 1: delay auxin From clkbuf	R/W	0
	RegDPCDReset	5	0: Normal 1: Reset DPCD FIFO	R/W	0
	RegdisSelAudID	4	Disable select Audio Stream ID	R/W	0
	Reg_newpkt_sel	3	New packet select	R/W	0
	RegCmd_Filttap	2	Setting for I2C salve	R/W	0
	RegCmd_Filttype	1	Setting for I2C salve	R/W	0
	RegCmd_Deglitch	0	Setting for I2C salve	R/W	0
35	RegNoInfothresh	7:4	No InfoFrame threshold	R/W	1000
	RegNoVideo	3	Software video mute value	R/W	0
	RegNoVideoEn	2	Software video mute enable	R/W	0
	RegAmute	1	Software audio mute value	R/W	0
	RegAmuteEn	0	Software audio mute enable	R/W	0
36	RegMajor_thresh	7:5	Majority allow continuous error threshold Maximum: 100	R/W	100
	RegECC_thresh	4:2	Error correction allow continuous error threshold per lane Maximum: 100	R/W	100
	RegDisECC	1	Disable secondary data RS ECC	R/W	0
	RegInvFieldEn	0	Video field top signal invert enable	R/W	0
37	Reg_PktRec_type	7:0	General packet type select	R/W	00000000
38	RegSelAudID	7:0	Audio stream ID select	R/W	00000000
3F	LSPkt_Type[7:0]	7:0	Received packet type[7:0] pulse	R1C	
40	Reserved	7:2	----------	RO	
	LSPkt_Type[9:8]	1:0	Received packet type[9:8] pulse	R1C	
41	LSAVIPktID	7:0	AVI InfoFrame packet ID	RO	
42	LSAVIDataCnt[7:0]	7:0	AVI InfoFrame data byte count[7:0]	RO	
43	LSAVIDPVer	7:2	AVI InfoFrame DP support version	RO	
43	LSAVIDataCnt[9:8]	1:0	AVI InfoFrame data byte count[9:8]	RO	
44	LSAVI1PB	7:0	AVI InfoFrame packet payload byte 1	RO	
45	LSAVI2PB	7:0	AVI InfoFrame packet payload byte 2	RO	

46	LSAVI3PB	7:0	AVI InfoFrame packet payload byte 3	RO	
47	LSAVI4PB	7:0	AVI InfoFrame packet payload byte 4	RO	
48	LSAVI5PB	7:0	AVI InfoFrame packet payload byte 5	RO	
49	LSAVI6PB	7:0	AVI InfoFrame packet payload byte 6	RO	
4A	LSAVI7PB	7:0	AVI InfoFrame packet payload byte 7	RO	
4B	LSAVI8PB	7:0	AVI InfoFrame packet payload byte 8	RO	
4C	LSAVI9PB	7:0	AVI InfoFrame packet payload byte 9	RO	
4D	LSAVI10PB	7:0	AVI InfoFrame packet payload byte 10	RO	
4E	LSAVI11PB	7:0	AVI InfoFrame packet payload byte 11	RO	
4F	LSAVI12PB	7:0	AVI InfoFrame packet payload byte 12	RO	
50	LSAVI13PB	7:0	AVI InfoFrame packet payload byte 13	RO	
51	LSSPDPktID	7:0	SPD InfoFrame packet ID	RO	
52	LSSPDDataCnt[7:0]	7:0	SPD InfoFrame data byte count[7:0]	RO	
53	LSSPDDPVer	7:2	SPD InfoFrame DP support version	RO	
	LSSPDDataCnt[9:8]	1:0	SPD InfoFrame data byte count[9:8]	RO	
54	LSSPD25PB	7:0	SPD InfoFrame packet payload byte 25	RO	
55	LSAudPktID	7:0	Audio InfoFrame packet ID	RO	
56	LSAudDataCnt[7:0]	7:0	Audio InfoFrame data byte count[7:0]	RO	
57	LSAudDPVer	7:2	Audio InfoFrame DP support version	RO	
	LSAudDataCnt[9:8]	1:0	Audio InfoFrame data byte count[9:8]	RO	
58	LSAud1PB	7:0	Audio InfoFrame packet payload byte 1	RO	
59	LSAud2PB	7:0	Audio InfoFrame packet payload byte 2	RO	
5A	LSAud3PB	7:0	Audio InfoFrame packet payload byte 3	RO	
5B	LSAud4PB	7:0	Audio InfoFrame packet payload byte 4	RO	
5C	LSAud5PB	7:0	Audio InfoFrame packet payload byte 5	RO	
5D	LSMpegPktID	7:0	Mpeg InfoFrame packet ID	RO	
5E	LSMpegDataCnt[7:0]	7:0	Mpeg InfoFrame data byte count[7:0]	RO	
5F	LSMpegDPVer	7:2	Mpeg InfoFrame DP support version	RO	
	LSMpegDataCnt[9:8]	1:0	Mpeg InfoFrame data byte count[9:8]	RO	
60	LSMpeg1PB	7:0	Mpeg InfoFrame packet payload byte 1	RO	
61	LSMpeg2PB	7:0	Mpeg InfoFrame packet payload byte 2	RO	
62	LSMpeg3PB	7:0	Mpeg InfoFrame packet payload byte 3	RO	
63	LSMpeg4PB	7:0	Mpeg InfoFrame packet payload byte 4	RO	
64	LSMpeg5PB	7:0	Mpeg InfoFrame packet payload byte 5	RO	
65	LSGenPkt_0HB	7:0	General packet header byte 0	RO	
66	LSGenPkt_1HB	7:0	General packet header byte 1	RO	
67	LSGenPkt_2HB	7:0	General packet header byte 2	RO	
68	LSGenPkt_3HB	7:0	General packet header byte 3	RO	
69	LSGenPkt_0pb	7:0	General packet payload byte 0	RO	
6A	LSGenPkt_1pb	7:0	General packet payload byte 1	RO	
6B	LSGenPkt_2pb	7:0	General packet payload byte 2	RO	
6C	LSGenPkt_3pb	7:0	General packet payload byte 3	RO	
6D	LSGenPkt_4pb	7:0	General packet payload byte 4	RO	
6E	LSGenPkt_5pb	7:0	General packet payload byte 5	RO	
6F	LSGenPkt_6pb	7:0	General packet payload byte 6	RO	
70	LSGenPkt_7pb	7:0	General packet payload byte 7	RO	
71	LSGenPkt_8pb	7:0	General packet payload byte 8	RO	
72	LSGenPkt_9pb	7:0	General packet payload byte 9	RO	
73	LSGenPkt_10pb	7:0	General packet payload byte 10	RO	
74	LSGenPkt_11pb	7:0	General packet payload byte 11	RO	
75	LSGenPkt_12pb	7:0	General packet payload byte 12	RO	
76	LSGenPkt_13pb	7:0	General packet payload byte 13	RO	
77	LSGenPkt_14pb	7:0	General packet payload byte 14	RO	
78	LSGenPkt_15pb	7:0	General packet payload byte 15	RO	
79	LSGenPkt_16pb	7:0	General packet payload byte 16	RO	
7A	LSGenPkt_17pb	7:0	General packet payload byte 17	RO	
7B	LSGenPkt_18pb	7:0	General packet payload byte 18	RO	
7C	LSGenPkt_19pb	7:0	General packet payload byte 19	RO	
7D	LSGenPkt_20pb	7:0	General packet payload byte 20	RO	
7E	LSGenPkt_21pb	7:0	General packet payload byte 21	RO	
7F	LSGenPkt_22pb	7:0	General packet payload byte 22	RO	
80	LSGenPkt_23pb	7:0	General packet payload byte 23	RO	

81	LSGenPkt_24pb	7:0	General packet payload byte 24	RO	
82	LSGenPkt_25pb	7:0	General packet payload byte 25	RO	
83	LSGenPkt_26pb	7:0	General packet payload byte 26	RO	
84	LSGenPkt_27pb	7:0	General packet payload byte 27	RO	
85	LSAudTStpPktID	7:0	Audio time stamp packet ID	RO	
86	LSAudTStpDCnt[7:0]	7:0	Audio time stamp data byte count[7:0]	RO	
87	LSAudTStpDPVer	7:2	Audio time stamp DP support version	RO	
	LSAudTStpDCnt[9:8]	1:0	Audio time stamp data byte count[9:8]	RO	
88	LSAudStrID	7:0	Audio stream packet ID	RO	
89	Reserved	7	----------	RO	
	LSAudStrCType	6:3	Audio stream coding type	RO	
	LSAudStrChCnt	2:0	Audio stream channel count	RO	
8A	LSMVid[7:0]	7:0	Mvid value[7:0] (don't care if novideo or video not ready)	RO	
8B	LSMVid[15:8]	7:0	Mvid value[15:8]	RO	
8C	LSMVid[23:16]	7:0	Mvid value[23:16]	RO	
8D	LSNVid[7:0]	7:0	Nvid value[7:0] (don't care if novideo or vide not ready)	RO	
8E	LSNVid[15:8]	7:0	Nvid value[15:8]	RO	
8F	LSNVid[23:16]	7:0	Nvid value[23:16]	RO	
90	LSMaud[7:0]	7:0	Maud value[7:0] (don't care if audmute)	RO	
91	LSMaud[15:8]	7:0	Maud value[15:8]	RO	
92	LSMaud[23:16]	7:0	Maud value[23:16]	RO	
93	LSNaud[7:0]	7:0	Naud value[7:0] (don't care if audmute)	RO	
94	LSNaud[15:8]	7:0	Naud value[15:8]	RO	
95	LSNaud[23:16]	7:0	Naud value[23:16]	RO	
96	LSAudID	7:0	Audio stream real-time ID, include : Audio InfoFrame Audio time stamp Audio stream	RO	
97	LSHTotal [7:0]	7:0	H total [7:0]	RO	
98	LSHTotal [15:8]	7:0	H total [15:8]	RO	
99	LSHStart[7:0]	7:0	H start [7:0] from Hsync start edge to H active start edge	RO	
9A	LSHStart[15:8]	7:0	H start [15:8] from Hsync start edge to H active start edge	RO	
9B	LSHWidth[7:0]	7:0	Main stream attribute data - H active width [7:0]	RO	
9C	LSHWidth[15:8]	7:0	Main stream attribute data -H active width [15:8]	RO	
9D	LSVTotal[7:0]	7:0	Main stream attribute data -V total [7:0]	RO	
9E	LSVTotal[15:8]	7:0	Main stream attribute data -V total [15:8]	RO	
9F	LSVStart[7:0]	7:0	Main stream attribute data -V start [7:0] from Vsync start edge to V active start edge	RO	
A0	LSVStart[15:8]	7:0	Main stream attribute data -V start [15:8] from Vsync start edge to V active start edge	RO	
A1	LSVHeight[7:0]	7:0	Main stream attribute data -V active height [7:0]	RO	
A2	LSVHeight[15:8]	7:0	Main stream attribute data -V active height [15:8]	RO	
A3	LSHSyncWidth[7:0]	7:0	Main stream attribute data -H Sync Width [7:0]	RO	
A4	LSHSyncPolarity	7	Main stream attribute data -H Sync polarity	RO	
	LSHSyncWidth[14:8]	6:0	Main stream attribute data -H Sync Width[14:8]	RO	
A5	LSVSyncWidth	7:0	Main stream attribute data -V Sync Width [7:0]	RO	
A6	LSVSyncPolarity	7	Main stream attribute data -VSync polarity	RO	
	LSVSyncWidth	6:0	Main stream attribute data -V Sync Width[14:8]	RO	
A7	LSVdBPC	7:5	Main stream attribute data -Bit depth per color / component 000 = 6 bits 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 16 bits 101, 110, 111 = Reserved	RO	
	LSVdYUVColor	4	Main stream attribute data -YCbCr Colorietry 0: ITU-R BT601-5 1: ITU-R BT709-5	RO	

	LSVdRange	3	Main stream attribute data -Dynamic range 0: VESA range (from 0 to the maximum) 1: CEA range	RO	
	LSVdPxlFormat	2:1	Main stream attribute data -Component format 00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 11: Reserved	RO	
	LSCLKSync	0	Main stream attribute data -Synchronous clock 0: Link clock and stream clock asynchronous 1: Link clock and stream clock synchronous	RO	
A8	Reserved	7:3	----------	RO	
	LSStereoVdAttr	2:1	Main stream attribute data -Stereo video attribute 00: No stereo video transported 01: for progressive vide, the next frame is RIGHT eye, for interlaced video, TOP field is RIGHT eye and BOTTOM field is LEFT eye 10: reserved and must not be used 11: for progressive video, the next frame is LEFT eye, for interlaced video, TOP field is LEFT eye and BOTTOM field is RIGHT eye	RO	
	LSVdIFrameEven	0	Main stream attribute data -Interlaced vertical total even 0: number of lines per interlaced frame (consisting of two fields) is an odd number 1: number of lines per interlaced frame (consisting of two fields) is an even number	RO	
A9	viditemcomp	7	Video format 5 attribute data compare bit-debug	RO	
	LSdiffVidFormat	6	Video main stream attribute data change	RO	
	LSHDCPSyncDet	5	HDCP SYNC DETECT	RO	
	LSAudMute	4	AudioMute_Flag	RO	
	LSNoVideo	3	NoVideoStream_Flag	RO	
	LSVdFrameMd	2	Interlace_Flag	RO	
	LSVdFieldTop	1	FieldID_Flag	RO	
	LSVBlank	0	VerticalBlanking_Flag	RO	
B0	RegOtpCtrl	7:0	Otp encryption word selection for EMemory data	R/W	00101010
B1	RegOtpXor	7:0	Otp XOR value for EMemory data	R/W	10100101
B2	RegEMemWeakRd	7	EMemory weak read	R/W	1
	RegEMemRWEn	6	EMemory Read/Write enable	R/W	1
	RegMasterSel	5	EMemory control master selection. 0: HDCP circuit. 1: Register control. (RegB3[7:4]~RegB6)	R/W	0
	RegROMBIST	4	ROM BIST enable (BIST function is not implemented, this bit is useless)	R/W	0
	RegEnEMem	3	EMemory enable	R/W	1
	RegPwrOnRdBksv	2	Automatically read Bksv when system power on	R/W	1
	RegDisDecryp	1	HDCP decryption disable	R/W	0
	RegCPDesired	0	HDCP enable	R/W	0
B3	RegDDCReq	7:4	Ememory DDC request command type. 0000: DDC request is valid. Others: invalid.	R/W	0000
	RegEMemLoad	3:0	EMemory load bit number. This setting extends the write enable pulse width for Ememory write. Unit: 1T I2C CLK.	R/W	0010
B4	RegDDCHeader	7:0	Ememory DDC Header. 11100000: EMemory DDC Read Bank0. 11100010: EMemory DDC Read Bank1. Others: invalid.	R/W	00000000
B5	RegDDCReqOffset	7:0	EMemory DDC Read Offset address.	R/W	00000000
B6	RegDDCReqByte	7:0	EMemory DDC request Byte Number.	R/W	00000000
B7	RegCRSymLockMax	7:0	Max number of locked symbol for Clock Recovery. Note: Due to the double size of bus width, the	R/W	01000000

			actual value is equal to the setting * 2.		
B8	RegCRSymLockMin	7:0	Min number of locked symbol for Clock Recovery. Note: Due to the double size of bus width, the actual value is equal to the setting * 2.	R/W	00100000
B9	RegEQSymLockMax	7:0	Max number of locked symbol for Channel Equalization. Note: Due to the double size of bus width, the actual value is equal to the setting * 2.	R/W	01000000
BA	RegEQSymLockMin	7:0	Min number of locked symbol for Channel Equalization. Note: Due to the double size of bus width, the actual value is equal to the setting * 2.	R/W	00100000
BB	RegCRTimer[7:0]	7:0	CR timeout Timer [7:0] Unit: 1 LSCLK period The number of the valid CR symbol must reach RegCRSymLockMax within this time period.	R/W	10100100
BC	RegEQTimer[7:0]	7:0	EQ timeout Timer [7:0] Unit: 1 LSCLK period The number of the valid EQ symbol must reach RegCRSymLockMax within this time period.	R/W	10100000
BD	RegSymLockMax	7:6	Max number of symbol lock for decreasing the number of lose symbol lock	R/W	00
	RegDisTxSense	5	Disable 1.1a Tx Sense function	R/W	0
	RegEnLaneSwp	4	Enable lane swap	R/W	0
	RegEQTimer[10:8]	3:1	EQ timeout Timer [10:8]	R/W	001
	RegCRTimer[8]	0	CR timeout Timer [8]	R/W	0
C0	RegEQFalCRMax	7:4	Max number of lost lock symbol in EQ phase. If the number of lost lock symbol exceeds this setting, CR_DONE in DPCD will be cleared. Unit: 16 times. Default value 0000 = 16 times.	R/W	0000
	RegSymUnLockMax	3:0	Max number of lost lock symbol in normal operation (after a successful Link Training). If the number of lost lock symbol exceeds this setting, CR_DONE, CHANNEL_EQ_DONE and SYMBOL _LOCKED in DPCD will be cleared. Unit: 16 times. Default value 0000 = 16 times.	R/W	0000
C1	RegCDRSel	7	AFE configuration value selection for Clock Recovery 1: analog CDR, 0:digital CDR	R/W	1
	Reserved	6		R/W	0
	RegSymAlignMax	5:4	Max number of symbol alignment for decreasing the number of lost symbol alignment in normal operation (after a successful Link Training). When the number of symbol alignment reaches this setting, subtract 1 from the number of lost symbol alignment. 00: 2^10 01: 2^12 10: 2^14 11: 2^16	R/W	00
	RegSymUnAlgnMax	3:0	Max number of lost symbol alignment in normal operation (after a successful Link Training). If the number of lost symbol alignment exceeds this setting, LANE_ALIGN_STATUS_UPDATED in DPCD will be cleared. Unit: 1 time. Default value 0001 = 1 time.	R/W	0001
C2	RegHPDIrqPeriod[7:0]	7:0	HPD Interrupt pulse period [7:0]. RegHPDIrqPeriod[11:0] is the time base. Unit: 37.04ns Default value 101010001010 is 100us.	R/W	10001010
C3	RegHPDIrqPeriod[15:8]	7:0	HPD Interrupt period [15:8] RegHPDIrqPeriod[15:12] is the time counter.	R/W	01011010

			Unit: time base defined in [11:0] Default value 0101 is 500us.		
C8	Reserved	7:6	----------		
	RegLnkTrnFail	5	Link Training fail status	RO	
	RegTxSense	4	Tx Sense status	RO	
	RegTxPwrSense	3	Tx power is on	RO	
	RegTxConnected	2	Tx is connected	RO	
	RegLnkTrnDn	1	Link Training done status	RO	
	RegLnkTrnBusy	0	Link Training busy status	RO	
C9	RegEnLaneNo	7:6	Lane enable in PHY test 00: lane0 01: lane1 10: lane2 11: lane3	R/W	00
	RegEnPHYTest	5	Enable PHY test	R/W	0
	RegEnHPDOut	4	Enable HPD output	R.W	0
	RegEnCRWait	3	Enable wait function in CR	R/W	0
	RegEnEQOpt	2	Enable optimization in EQ	R/W	0
	RegEnCROpt	1	Enable optimization in CR	R/W	0
	RegAutoDSkwEn	0	Enable inter-lane and H/L byte De-Skew	R/W	0
CC	RegCRTimeBase[3:0]	7:4	Time base for CR wait function. RegCRTimeBase[11:0] is the time base. Unit: 37.04ns Default value 101011101000 is 100us.	R/W	1000
	RegCRWaitCnt	3:0	Time counter for CR wait function Unit: time base defined in RegCRTimeBase[11:0] Default value 0001 is 100us.	R/W	0001
CD	RegCRTimeBase[11:4]	7:0	Time base for CR wait function. RegCRTimeBase[11:0] is the time base. Unit: 37.04ns Default value 101011101000 is 100us.	R/W	10101110
CE	RegSetLnkStUpd	7	Force LINK_STATUS_UPDATED in DPCD	R/W	0
	RegDBounceTime	6:3	Tx sense and Tx connected de-bounce time Unit: 150us Default value 0000 is 150us.	R/W	0000
	RegDisTrnVELmt	2	Disable Link Training 1.2V limitation	R/W	0
	RegEnEQTimer	1	Enable EQ timeout timer	R/W	0
	RegEnCRTimer	0	Enable CR timeout timer	R/W	0
CF	RegSetRepeater	2	Enable HDCP repeater function	R/W	0
	RegForceVReady	1	Force V' Ready in DPCD	R/W	0
	RegForceCPRdy	0	Force CP Ready in DPCD	R/W	0
D0		7:0		R/W	00000101
D1		7:4		R/W	0000
		3		R/W	1
		2:0		R/W	000
D2		7:6		R/W	00
		5		R/W	0
	RegAttrSet	4	Set main stream attribute from RegD3 ~ RegE2	R/W	0
		3		R/W	0
		2		R/W	0
		1:0		R/W	00
D3	RegHWidth[7:0]	7:0	H active width [7:0]	R/W	00000000
D4	RegHWidth[15:8]	7:0	H active width [15:8]	R/W	00000000
D5	RegHTotal[7:0]	7:0	H total [7:0]	R/W	00000000
D6	RegHTotal[15:8]	7:0	H total [15:8]	R/W	00000000
D7	RegHStart[7:0]	7:0	H start [7:0] from Hsync start edge to H active start edge	R/W	00000000
D8	RegHStart[15:8]	7:0	H start [15:8] from Hsync start edge to H active start edge	R/W	00000000
D9	RegHSyncWidth[7:0]	7:0	H Sync Width [7:0]	R/W	00000000
DA	RegVdHSyncP	7	H Sync polarity	R/W	0
	RegHSyncWidth[14:8]	6:0	H Sync Width[14:8]	R/W	0000000
DB	RegVTotal[7:0]	7:0	V total [7:0]	R/W	00000000

DC	RegVTotal[15:8]	7:0	V total [15:8]	R/W	00000000
DD	RegVHeight[7:0]	7:0	V active height [7:0]	R/W	00000000
DE	RegVHeight[15:8]	7:0	V active height [15:8]	R/W	00000000
DF	RegVStart[7:0]	7:0	V start [7:0] from Vsync start edge to V active start edge	R/W	00000000
E0	RegVStart[15:8]	7:0	V start [15:8] from Vsync start edge to V active start edge	R/W	00000000
E1	RegVSyncWidth[7:0]	7:0	V Sync Width [7:0]	R/W	00000000
E2	RegVdVSyncP	7	VSync polarity	R/W	0
	RegVSyncWidth[14:8]	6:0	V Sync Width[14:8]	R/W	0000000
E3	RegVBlankGen	7		R/W	0
	RegPatBIn	6		R/W	0
	RegPatIn	5		R/W	0
	RegPatGenEn	4		R/W	0
	RegDisOUFlow	3		R/W	0
	RegDisUpDown	2		R/W	0
	RegIntOutType	1	Interrupt Out Type 0: Push/Pull 1: open drain	R/W	0
	RegIntPol	0	Interrupt Polarity selection	R/W	0
E4	RegIntMask[7:0]	7:0	Interrupt Mask [7:0] For register 07 (one to one mapping)	R/W	11111111
E5	RegIntMask[15:8]	7:0	Interrupt Mask [15:8] For register 08	R/W	11111111
E6	RegIntMask[23:16]	7:0	Interrupt Mask [23:16] For Register 09	R/W	11111111
E7	RegIntMask[31:24]	7:0	Interrupt Mask [31:24] For Register 0A	R/W	11111111
E8	RegIntMask[39:32]	7:0	Interrupt Mask [39:32] For Register 0B	R/W	11111111
E9	RegIntMask[47]	7	Reserved For future use	R/W	1
	RegIntMask[46:40]	6:0	For Resister 0C[6:0]	R/W	1111111
EA	RegDeMUXRST	7	DeMUX module reset	R/W	0
	RegLKTrainRST	6	LinkTrain module reset	R/W	0
	RegHDCPRST	5	HDCP module reset	R/W	0
	RegRRST	4	Register module reset	R/W	0
	RegAUXRST	3	AUX Channel reset	R/W	0
	RegAudRST	2	Audio module reset	R/W	0
	RegVidRST	1	Video module reset	R/W	0
	RegSWRST	0	Software reset	R/W	0
EB	RegLSCKInv	7	LSCLK inverse	R/W	0
	RegPWDTOP	6	Power down all digital block	R/W	0
	RegTriVDIO	5	Turn off Video Data IO (Set Tri-state)	R/W	0
	RegTriVIO	4	Turn off Video Control signal (Vsync, Hsync, DE, Pixel CLK)	R/W	0
	RegTriSPDIF	3	Turn off Audio SPDIF I/O	R/W	0
	RegTriI2SB	2	Turn off Audio I2S channel3~8 I/O	R/W	0
	RegTriI2SA	1	Turn off Audio I2S channel1~2, control I/O	R/W	0
	RegAutoAUXRST	0	'1' : Enable AUX Auto Reset	R/W	0
EC	RegAUXFreqLock	7		RO	
	RegXCLKerr	6		RO	

	RegFixedAuxFreq	5		R/W	0
	RegOSCSel	4	0: OSCLKI 1: RING27M	R/W	0
	RegCK54Sel	3	0: through PLL 1: not through PLL	R/W	0
	RegAuxFilterNum	2:1		R/W	00
	RegOSCOCLKSel	0	0: XCLK 1: not XCLK XCLK=27MHz from CK54M for Mbus	R/W	0
ED	RegPWDVDual	7	Power down Dual pixel mode path	R/W	0
	RegPWDCSC	6	Power single pixel mode path	R/W	0
	Reserved	5	B2 Revision	RO	
	RegAuxFreqSet	4:0		R/W	01100
EE	RegTriVDIO	7:2	Trun off Video data bus [7:5]: control QB bus (3 components) [4:2]: control QA bus (3 components)	R/W	000000
	RegEnDebug	1		R/W	0
	RegPWDAudio	0	Power down Audio function block	R/W	0
EF	Reserved	7		RO	
	Reg656Swap	6		R/W	0
	RegPclkBInv	5		R/W	0
	RegPclkBDly	4:3		R/W	00
	RegDclkInv	2	Output Pixel clock phase inverse	R/W	0
	RegDclkDly	1:0	Output Pixel clock delay 00: no delay 01: delay 1ns 10: delay 2ns 11: delay 3ns	R/W	00
F0	RegPCLKOSel	7	0: PCLKO = PCLK 1: PCLKO = not PCLK	R/W	0
	RegErrCntDiv	6:5	00: div 1, 01: div 2, 10: div 4, 11: div 8	R/W	00
	RegNormalCnt	4	1: enable 8b/10b error counter when normal state 0: disable 8b/10b error counter when normal state	R/W	0
	RegErrThreshold	3:0	Error bit threshold for PRBS test	R/W	0000
F1	RegEnTest	7	NLPCM	R/W	0
	RegMBusSel	6	0: write 4 link train data words to register 1: write 3 link train data words to register	R/W	0
	RegMBusCnt	5:2	The period that write link train data to register	R/W	1010
	RegLkErrCntRst	1	1: Force Reset Link Test Counter	R/W	0
	RegEnErrCntDiv	0	0: disable link test error count division 1: enable link test error count division	R/W	0
F4	RegAMavgCnt[7:0]	7:0		R/W	00000110
F5	RegAMinimode	7		R/W	1
	RegSSCAFrange	6:3		R/W	0000
	RegAMavgCnt[10:8]	2:0		R/W	000
F6	RegWs_sel	7	I2S word select switch 0: left -> right, 1:right->left	R/W	0
	RegACINC	6		R/W	0
	RegMCLKSel	5:4		R/W	01
	RegARDec	3:2		R/W	00
	RegAPLLGain	1:0		R/W	01
F7	RegI2s_mode	7:6	I2S mapping mode select 00:i2s, 01:right, 10:left, 11:raw 60958	R/W	00
	RegAudVolCtrl	5:4	Audio volume control	R/W	00

	RegHWAudMuteClrMode	3	Audio hardware mute clear enable	R/W	0
	RegBiphasemode	2	SPDIF output enable	R/W	0
	RegHWMuteClr	1	Audio hardware mute clear	R/W	0
	RegHWMuteEn	0	Audio hardware mute enable	R/W	0
F8	RegI2S_CH3SEL	7:6	I2S channel 3 output source select	R/W	11
F8	RegI2S_CH2SEL	5:4	I2S channel 2 output source select	R/W	10
	RegI2S_CH1SEL	3:2	I2S channel 1 output source select	R/W	01
	RegI2S_CH0SEL	1:0	I2S channel 0 output source select	R/W	00
F9	RegHWMuteRate[7:0]	7:0	Audio hardware mute rate low byte	R/W	00100000
FA	RegI2s_width	7:3	I2S word length select	R/W	11000
	RegHWMuteRate[10:8]	2:0	Audio hardware mute rate high bits	R/W	000
FB	Reserved	7:6	----------	RO	
	RegFSdec	3:0		RO	
FC	RegI2CStCnt	7:0	Set I2C SCL frequency	R/W	00100001
FD	Reserved	7:4	----------		
	RegCheckAudMute	3	Check audio mute or not for Maud, Naud	R/W	0
	RegI2CRdDiffer	2	0: Ack Mode 1: differ mode	R/W	0
	RegI2CModelSel	1	Enable Internal EDID access	R/W	0
	Reg1usCntX2En	0	Enable 1us count double number	R/W	0

Bank 1 : Reg05[3][0] = '0' '1'

Reg	Register Name	Bit	Definition	Type	Default Value
10	DPCD100H		Internal DPCD100H value		
11	DPCD101H		Internal DPCD101H value		
12	DPCD102H		Internal DPCD102H value		
13	DPCD103H		Internal DPCD103H value		
14	DPCD104H		Internal DPCD104H value		
15	DPCD105H		Internal DPCD105H value		
16	DPCD106H		Internal DPCD106H value		
17	DPCD107H		Internal DPCD107H value		
18	DPCD108H		Internal DPCD108H value		
19	DPCD200H		Internal DPCD200H value		
1A	DPCD202H		Internal DPCD202H value		
1B	DPCD203H		Internal DPCD203H value		
1C	DPCD204H		Internal DPCD204H value		
1D	DPCD205H		Internal DPCD205H value		
1E	DPCD206H		Internal DPCD206H value		
1F	DPCD207H		Internal DPCD207H value		
20	DPCD210H		Internal DPCD210H value		
21	DPCD211H		Internal DPCD211H value		
22	DPCD212H		Internal DPCD212H value		
23	DPCD213H		Internal DPCD213H value		
24	DPCD214H		Internal DPCD214H value		
25	DPCD215H		Internal DPCD215H value		
26	DPCD216H		Internal DPCD216H value		
27	DPCD217H		Internal DPCD217H value		
28	RegDPCD100h	7:0	Force value for DPCD100H	R/W	00000110
29	RegDPCD101h	7:0	Force value for DPCD101H	R/W	00000001
2A	RegDPCD102h	7:0	Force value for DPCD102H	R/W	00000000
2B	RegDPCD103h	7:0	Force value for DPCD103H	R/W	00000000
2C	RegDPCD104h	7:0	Force value for DPCD104H	R/W	00000000
2D	RegDPCD105h	7:0	Force value for DPCD105H	R/W	00000000
2E	RegDPCD106h	7:0	Force value for DPCD106H	R/W	00000000
2F	RegDPCD107h	7:0	Force value for DPCD107H	R/W	00000000
30~6A	hdcp68000 ~ hdcp6803A		Internal DPCD68000~6803A values		
70	Reg_LMSwap	7	1: swap output direction(MSB/LSB)	R/W	0
	Reg_O16Bit	6	'1' : YCbCr422 output only 16bit width '0': YCbCr422 output is 24/20 bit width.	R/W	0
	Reg_OUTBit	5:4	00: output 8 bits per color channel 01:output 10 bits per color channel 10:output 12 bits per color channel 11: reserved	R/W	00
	Reg_ColorDepth	3:2	00: output 8 bits 444 format 01: output 10 bits 444 format 10: output 12 bits 444 format	R/W	01
	Reg_PCLKDiv2	1	'1': output half PCLK	R/W	0
	Reg_ChgSyncPol	0	'1': output H/V sync indicated by reg171[2]/reg171[3] '0': keep the original sync polarity.	R/W	0
71	Reg_PGEn	7	reserved	R/W	0
	Reg_DNFreeGo	6	'1': Dither free go.	R/W	0
	Reg_EnUdFilt	5	'1': Enable 444 ↔ 422 up/down filter	R/W	0
	Reg_EnDither	4	'1': Enable Dither	R/W	0
	Reg_VSyncPol	3	'1': Set V sync polarity as positive while reg170[0] as '1' '0': Set V sync polarity as negative while reg170[0] as '1'	R/W	0

	Reg_HSyncPol	2	'1': Set H sync polarity as positive while reg170[0] as '1' '0': Set YH sync polarity as negative while reg170[0] as '1'	R/W	0
	Reg_ChSwap	1	'1': Swap output R/B(Cr/Cb) channel	R/W	0
	Reg_RBSwap	0	'1': Swap input R/B(Cr/Cb) channel	R/W	0
72	Reserve	7:6		R/W	00
	Reserve	5:4		R/W	00
	Reserve	3:2		R/W	00
	Reg_HDMIColMod	1:0		R/W	00
73	Reg_YOffSet	7:0		R/W	00000000
74	Reg_COffSet	7:0		R/W	00000000
75	Reg_RGBOffSet	7:0		R/W	00000000
176	Reg_PGVMD	7:6		R/W	00
	Reg_PGHMD	5:4		R/W	00
	Reg_SyncEmb	3		R/W	0
	Reg_PGVRep2	2		R/W	0
	Reg_PGHRep2	1		R/W	0
	Reg_PGFreeGo	0		R/W	0
77	Reg_PGColR	7:0	Pattern generator R data	R/W	00000000
78	Reg_PGColG	7:0	Pattern generator G data	R/W	00000000
79	Reg_PGColB	7:0	Pattern generator B data	R/W	00000000
7A	Reg_PGColBlank	7:0		R/W	00000000
7B	Reg_PGColBlankY	7:0		R/W	00000000
7C	Reg_PGHActSt[7:0]	7:0	Horizontal active start low byte for PGDataPro module	R/W	10001001
7D	Reg_PGHActEd[7:0]	7:0	Horizontal active end low byte for PGDataPro module	R/W	01011001
7E	Reg_PGHActEd{11:8}	7:4	Horizontal active end high bits for PGDataPro module	R/W	0011
	Reg_PGHActSt[11:8]	3:0	Horizontal active start high bits for PGDataPro module	R/W	0000
7F	Reg_PGVActSt[7:0]	7:0	Vertical active start low byte for PGDataPro module	R/W	00100011
80	Reg_PGVActEd[7:0]	7:0	Vertical active end low byte for PGDataPro module	R/W	00000011
81	Reserved	7	----------		
	Reg_FastMode	6	Fast simulation mode enable	R/W	0
	Reg_PGVActEd[10:8]	5:3	Vertical active end high bits for PGDataPro module	R/W	010
	Reg_PGVActSt[10:8]	2:0	Vertical active start high bits for PGDataPro module	R/W	000
82	Reg_PGVActSt2nd[7:0]	7:0		R/W	11111111
83	Reg_PGVActEd2nd[7:0]	7:0		R/W	11111111
84	Reg_PGVActEd2nd[10:8]	5:3		R/W	111
	Reg_PGVActSt2nd[10:8]	2:0		R/W	111
85	Reg_PGHTotal[7:0]	7:0	Horizontal total low byte for PGDataPro module	R/W	01011001
86	Reg_PGHSyncSt[7:0]	7:0	Horizontal sync start low byte for PGDataPro module	R/W	00001111
87	Reg_PGHSyncSt[11:8]	7:4	Horizontal sync start high bits for PGDataPro module	R/W	0000
	Reg_PGHTotal[11:8]	3:0	Horizontal total high bits for PGDataPro module	R/W	0011
88	Reg_PGHSyncEd[7:0]	7:0	Horizontal sync end low byte for PGDataPro module	R/W	01001101
89	Reg_PGVSyncEd	4:1	Vertical sync end bit for PGDataPro module	R/W	0101
	Reg_PGHSyncEd[8]	0	Horizontal sync end high bit for PGDataPro module	R/W	0
8A	Reg_PGVTotal[7:0]	7:0	Vertical total low byte for PGDataPro module	R/W	00001100
8B	Reg_PGVSyncSt[7:0]	7:0	Vertical sync start low byte for PGDataPro module	R/W	00001100
8C	Reg_PGVSyncSt[10:8]	5:3	Vertical sync start high bits for PGDataPro module	R/W	010
	Reg_PGVTotal[10:8]	2:0	Vertical total high bits for PGDataPro module	R/W	010
8D	Reg_PGCHInc	7:0		R/W	00010000
8E	Reg_PGCVInc	7:0		R/W	00010000
8F	Reg_OutDDR	7	'1': Output bus width is half and trigger data under dual edge.	R/W	0
	Reg_2x656Clk	6	'1': Output CCIR656 data with twice PCLK.	R/W	0
	Reg_656FFRst	5	'1': reset 656 FIFO. '0': resume Under CCIR656 mode, set the bit then clear it before unmute the output.	R/W	0
	Reg_EnAVMuteRst	4	'1': Enable Auto AVMUTE reset.	R/W	0

	Reg_CSCSel	3:2	Color space conversion select 0x: CSC disable 10: RGB to YUV, 11:YUV to RGB	R/W	00
	Reg_OutColMod	1:0	00: RGB444 mode 01: YCbCr422 mode 10: YCbCr444 mode.	R/W	10
90	Reg_Matrix11V[7:0]	7:0	CSC matrix 11 low byte	R/W	10110010
91	Reserved	7:6	----------	RO	
	Reg_Matrix11V[13:8]	5:0	CSC matrix 11 high bits	R/W	000100
92	Reg_Matrix12V[7:0]	7:0	CSC matrix 12 low byte	R/W	01100100
93	Reserved	7:6	----------	RO	
	Reg_Matrix12V[13:8]	5:0	CSC matrix 12 high bits	R/W	000010
94	Reg_Matrix13V[7:0]	7:0	CSC matrix 13 low byte	R/W	11101001
95	Reserved	7:6	----------	RO	
	Reg_Matrix13V[13:8]	5:0	CSC matrix 13 high bits	R/W	000000
96	Reg_Matrix21V[7:0]	7:0	CSC matrix 21 low byte	R/W	10010011
97	Reserved	7:6	----------	RO	
	Reg_Matrix21V[13:8]	5:0	CSC matrix 21 high bits	R/W	011100
98	Reg_Matrix22V[7:0]	7:0	CSC matrix 22 low byte	R/W	00010110
99	Reserved	7:6	----------	RO	
	Reg_Matrix22V[13:8]	5:0	CSC matrix 22 high bits	R/W	000100
9A	Reg_Matrix23V[7:0]	7:0	CSC matrix 23 low byte	R/W	01010110
9B	Reserved	7:6	----------	RO	
	Reg_Matrix23V[13:8]	5:0	CSC matrix 23 high bits	R/W	011111
9C	Reg_Matrix31V[7:0]	7:0	CSC matrix 31 low byte	R/W	01001001
9D	Reserved	7:6	----------	RO	
	Reg_Matrix31V[13:8]	5:0	CSC matrix 31 high bits	R/W	011101
9E	Reg_Matrix32V[7:0]	7:0	CSC matrix 32 low byte	R/W	10011111
9F	Reserved	7:6	----------	RO	
	Reg_Matrix32V[13:8]	5:0	CSC matrix 32 high bits	R/W	011110
A0	Reg_Matrix33V[7:0]	7:0	CSC matrix 33 low byte	R/W	00010110
A1	Reserved	7:6	----------	RO	
	Reg_Matrix33V[13:8]	5:0	CSC matrix 33 high bits	R/W	000100
A2	Reserved	7:4	----------	RO	
	RegABSwap	3		R/W	0
	RegLMSwapB	2		R/W	0
	RegRBSwapB	1		R/W	0
	RegDualFFRst	0		R/W	0
A5	Reg_VCLK_ST0	7	Pixel CLK driving strength[0]	R/W	0
	Reg_VCLK_ST1	6	Pixel CLK driving strength[1]	R/W	0
	Reg_VCLK_ST2	5	Pixel CLK driving strength[2]	R/W	0
	Reg_VCLK_SLEW	4	Pixel CLK driving slew rate (1 = low slew)	R/W	0
	Reg_VIO_ST0	3	Video Data driving strength[0]	R/W	0
	Reg_VIO_ST1	2	Video Data driving strength[1]	R/W	0
	Reg_VIO_ST2	1	Video Data driving strength[2]	R/W	0
	Reg_VIO_SLEW	0	Video Data driving slew rate	R/W	0
A6	Reg_MCLK_ST0	7	Audio MCLK driving strength[0]	R/W	0
	Reg_MCLK_ST1	6	Audio MCLK driving strength[1]	R/W	0
	Reg_MCLK_ST2	5	Audio MCLK driving strength[2]	R/W	0
	Reg_MCLK_SLEW	4	Audio MCLK driving slew rate	R/W	0
	Reg_AIO_ST0	3	Audio Data driving strength[0]	R/W	0
	Reg_AIO_ST1	2	Audio Data driving strength[1]	R/W	0
	Reg_AIO_ST2	1	Audio Data driving strength[2]	R/W	0
	Reg_AIO_SLEW	0	Audio Data driving slew rate	R/W	0
A7	Reserved	7:6	----------	RO	
	Reg_DDCSDA_ST0	5		R/W	0
	Reg_DDCSDA_ST1	4		R/W	0
	Reg_DDCSDA_SLEW	3		R/W	0
	Reg_PCSDA_ST0	2		R/W	0
	Reg_PCSDA_ST1	1		R/W	0
	Reg_PCSDA_SLEW	0		R/W	0
A8	Reserved	7	----------	RO	

	RegAdien	6		R/W	0
	RegAdissdm	5		R/W	0
	RegPLLMCLKSel	4:2		R/W	001
	RegVdien	1		R/W	0
	RegVdissdm	0		R/W	0
B0	Reserved	7:4	----------	RO	
	CPLL_LOCK3	3	Indicate if the L3 CDR PLL is locked	RO	
	CPLL_LOCK2	2	Indicate if the L2 CDR PLL is locked	RO	
	CPLL_LOCK1	1	Indicate if the L1 CDR PLL is locked	RO	
	CPLL_LOCK0	0	Indicate if the L0 CDR PLL is locked	RO	
B1	Reserved	7	----------	RO	
	Reg_PWDL3	6	Power down lane 3	R/W	0
	Reg_PWDL2	5	Power down lane 2	R/W	0
	Reg_PWDL1	4	Power down lane 1	R/W	0
	Reg_PWDL0	3	Power down lane 0	R/W	0
	Reg_PWDAPLL	2	Power down Audio PLL	R/W	0
	Reg_PWDVPLL	1	Power down Video PLL	R/W	0
	Reg_PWDALL	0	Power down all blocks	R/W	0
B2	Reg_PWDCPLL[3]	7	Power down Lane3 Analog CDR PLL	R/W	0
	Reg_PWDCPLL[2]	6	Power down Lane2 Analog CDR PLL	R/W	0
	Reg_PWDCPLL[1]	5	Power down Lane1 Analog CDR PLL	R/W	0
	Reg_AUX_VSW	4		R/W	0
	Reg_PWDAUX	3	Power down AUX channel	R/W	0
	Reg_PWDCPLL[0]	2	Power down Lane0 Analog CDR PLL	R/W	0
	Reg_PWDIPLL_C	1	Current source bias generator powerdown Bar PWDB2=0 will put PLL's current source bias generator into power down mode.	R/W	0
	Reg_PWDIPLL	0	PLL powerdown PWDB=0 will put PLL into power down mode except current bias.	R/W	0
B3	Reg_RSTCDR	7	Reset digital CDR block	R/W	0
	Reg_RSTFIFO	6	Reset 8b/10b FIFO	R/W	0
	Reg_RSTAFE	5	Reset all AFE	R/W	0
	Reg_RSTCPLL	4	Reset CDR PLL	R/W	0
	Reg_RSTIPLL	3	Reset interpolation PLL	R/W	0
	Reg_RSTAPLL	2	Reset Audio PLL	R/W	0
	Reg_RSTVPLL	1	Reset Video PLL	R/W	0
	Reserved	0	----------	RO	
B4	Reg_PORT_EN	7:6	Not used	R/W	00
	Reg_OUT_SEL	5:4	Select output type on the video output 00: 20 bits mode 01: 8bits mode 10: 10bits mode 11: 20bits mode with lane inversion	R/W	00
	Reserved	3	----------	RO	
	Reg_CKSEL	2	Select CDR type 1: analog type 0: digital type	R/W	1
	Reg_DPENB	1	Enable display mode, low active; otherwise enable hdmi mode	R/W	0
	Reg_RBR	0	1: Reduced bit rate mode, 1.62G 0: High bit rate mode, 2.25G	R/W	0
B5	Reg_AFEBACKUP1	7		R/W	0
	Reg_AFEBACKUP0	6		R/W	0
	RegIPLL_ER0	5	ER0=1 increase filter resistance	R/W	0
	RegIPLL_GAIN	4	GAIN=1 increase VCO speed Set GAIN=0 ER0=1 and EC1=1 When output clock < 500MHz Set GAIN=1 ER0=0 and EC1=0 When output clock > 500MHz In DisplayPort Mode, Set GAIN=1 ER0=0	R/W	1
	RegIPLL_CP3	3	CDRPLL charge pump control registers Control the current size of ICR[3:0]	R/W	0
	RegIPLL_CP2	2		R/W	0
	RegIPLL_CP1	1		R/W	1

	RegIPLL_CP0	0		R/W	0
B7	RegCPLL_RPLLT3	7	Reserved	R/W	0
	RegCPLL_RPLLT2	6	Reserved	R/W	0
	RegCPLL_RPLLT1	5	DEK	R/W	1
	RegCPLL_RPLLT0	4	SWEN	R/W	1
	regcpll_ovwr	3	Force overwrite GAIN Otherwise according to RBR	R/W	0
	RegCPLL_KKENB	2		R/W	0
	RegCPLL_ER0	1	CPLL_ER0=1 increase digital damping R	R/W	0
	RegCPLL_Gain	0	Set Gain=1 when data rate is 2.7Gb/s Set Gain=0 when data rate is 1.62Gb/s	R/W	1
C0	Reg_train	7:4		R/W	0000
	RegL3_CPLL_ENPDB	3	0: when data is random 1: when data is D10.2 Note: for normal training, this bit must be set to 1 for clock recovery before changed to 0 for data recovery	R/W	1
	RegL2_CPLL_ENPDB	2		R/W	1
	RegL1_CPLL_ENPDB	1		R/W	1
	RegL0_CPLL_ENPDB	0		R/W	1
D1	Reg_ZR3_2nd	7		RW	
	Reg_ZR2_2nd	6		RW	
	Reg_ZR1_2nd	5		RW	
	Reg_ZR0_2nd	4		RW	
	Reg_LaneCkSel	3:2		R/W	00
	Reg_AUX_HYS1	1		R/W	0
	Reg_AUX_HYS0	0		R/W	0
E0	Reserved	7:4	----------	RO	
	RegPhyTestPtn	3	Set =1 to request the PHY test pattern as specified at DPCD address 00248h.	R/W	0
	RegTestEDIDRd	2	0: no EDID read test requested. 1: EDID read test requested.	R/W	0
	RegTestPtnReq	1	0: no test pattern requested. 1: test pattern requested.	R/W	0
	RegTestLkTrain	0	0: no link training test requested. 1: link training test requested.	R/W	0
E1	RegTestLkRate	7:0	06h : 1.62Gbps 0Ah: 2.7Gbps	R/W	00000110
E2	Reserved	7:5	----------	RO	
	RegTestLaneCnt	4:0	1h: one lane 2h: two lanes 4h: four lanes	R/W	00001
E3	M0[7:0]	7:0	M0 Byte0	RO	00000000
E4	M0[15:8]	7:0	M0 Byte1	RO	00000000
E5	M0[23:16]	7:0	M0 Byte2	RO	00000000
E6	M0[31:24]	7:0	M0 Byte3	RO	00000000
E7	M0[39:32]	7:0	M0 Byte4	RO	00000000
E8	M0[47:40]	7:0	M0 Byte5	RO	00000000
E9	M0[55:48]	7:0	M0 Byte6	RO	00000000
EA	M0[63:56]	7:0	M0 Byte7	RO	00000000
EB	RegTestVStart[7:0]	7:0	Vertical active start from Vsync start in line count	R/W	00000000
EC	RegTestHSyncPol	7	Test horizontal sync polarity	R/W	0
	RegTestHSyncWid[14:8]	6:0	Hsync width in pixel count	R/W	0000000
ED	RegTestHSyncWid[7:0]	7:0		R/W	00000000
EE	RegTestVSyncPol	7	Test vertical sync polarity	R/W	0
	RegTestVSyncWid[14:8]	6:0	Vsync width in line count	R/W	0000000
EF	RegTestVSyncWid[7:0]	7:0		R/W	00000000
F0	RegTestHWidth[15:8]	7:0	Active video width in pixel count	R/W	00000000
F1	RegTestHWidth[7:0]	7:0		R/W	00000000
F2	RegTestVHeight[15:8]	7:0	Active video height in line count	R/W	00000000
F3	RegTestVHeight[7:0]	7:0		R/W	00000000

F4	RegTestBitDepth	7:5	Bit depth per color 000: 6 bits 001: 8 bits 010: 10 bits 011: 12 bits 100: 16 bits others: reserved	R/W	000
	RegTestYCbCrCof	4	0: ITU601 1: ITU 709	R/W	0
	RegTestDRange	3	0: VESA range 1: CEA range	R/W	0
	RegTestColorFmt	2:1	00: RGB 01: YCbCr 4:2:2 10: YCbCr 4:4:4 11: reserved	R/W	00
	RegTestSyncClk	0	0: link clock and stream clock asynchronous 1: link clock and stream clock synchronous	R/W	0
F5	Reserved	7:2	----------	RO	
	RegTestIntLaced	1	0: non-interlaced 1: interlaced	R/W	0
	RegTestRefhDen	0	Test refresh denominator 0: 1 1: 1.001	R/W	0
F6	RegTestRefhRate	7:0	Indicates the refresh rate requested by the Sink Device.	R/W	00000000
F7	RegTestCRCRCr(7:0)	7:0	Stores the 16 bit CRC value of the R or Cr component.	R/W	00000000
F8	RegTestCRCRCr(15:8)	7:0		R/W	00000000
F9	RegTestCRCGY(7:0)	7:0	Stores the 16 bit CRC value of the G or Y component.	R/W	00000000
FA	RegTestCRCGY(15:8)	7:0		R/W	00000000
FB	RegTestCRCBCb(7:0)	7:0	Stores the 16 bit CRC value of the B or Cb component.	R/W	00000000
FC	RegTestCRCBCb(15:8)	7:0		R/W	00000000
FD	Reserved	7:5	----------	RO	
	RegTestCRCSup	4	0: CRC not supported by Sink Device 1: CRC supported by Sink Device	R/W	0
	RegTestCRCCnt	3:0	4 bit wrap counter which increments each time the reg1F7h~reg1FCh are updated. Reset to 0 when TEST_SINK bit 0 = 0.	R/W	0000
FE	Reserved	7:6	----------	RO	
	RegTestSinkStr	5	0: Stop calculating CRC on the next frame. 1: Start calculating CRC on the next frame.	RO	
	RegEDIDCkSumWr	4	0: no write to TEST_EDID_CHECKSUM 1: EDID checksum has been written to TEST_EDID_CHECKSUM	RO	
	RegTestNak	3	0: writing zero has no effect on TEST_REQ state 1: negative acknowledgement of TEST_REQ.	RO	
	RegTestAck	2	0: writing zero has no effect on TEST_REQ state 1: positive acknowledgement of TEST_REQ.	RO	
	RegPhyTPtnSel	1:0	00: No test pattern selected 01: D10.2 without scrambling 10: SERM 11: PRBS7	R/W	00
FF	RegEDIDCkSum	7:0	In the TEST_EDID mode, the checksum of the last EDID block that was read is written here.	RO	

Bank 2 : (reg5[3] = '1', reg5[0] = '0')

Reg	Register Name	Bit	Definition	Type	Default Value
210	KSV0FIFO[7:0]	7:0	KSV0FIFO Byte0	R/W	00000000
211	KSV0FIFO[15:8]	7:0	KSV0FIFO Byte1	R/W	00000000
212	KSV0FIFO[23:16]	7:0	KSV0FIFO Byte2	R/W	00000000
213	KSV0FIFO[31:24]	7:0	KSV0FIFO Byte3	R/W	00000000
214	KSV0FIFO[39:32]	7:0	KSV0FIFO Byte4	R/W	00000000
215	KSV1FIFO[7:0]	7:0	KSV1FIFO Byte0	R/W	00000000
216	KSV1FIFO[15:8]	7:0	KSV1FIFO Byte1	R/W	00000000
217	KSV1FIFO[23:16]	7:0	KSV1FIFO Byte2	R/W	00000000
218	KSV1FIFO[31:24]	7:0	KSV1FIFO Byte3	R/W	00000000
219	KSV1FIFO[39:32]	7:0	KSV1FIFO Byte4	R/W	00000000
21A	KSV2FIFO[7:0]	7:0	KSV2FIFO Byte0	R/W	00000000
21B	KSV2FIFO[15:8]	7:0	KSV2FIFO Byte1	R/W	00000000
21C	KSV2FIFO[23:16]	7:0	KSV2FIFO Byte2	R/W	00000000
21D	KSV2FIFO[31:24]	7:0	KSV2FIFO Byte3	R/W	00000000
21E	KSV2FIFO[39:32]	7:0	KSV2FIFO Byte4	R/W	00000000
21F	KSV3FIFO[7:0]	7:0	KSV3FIFO Byte0	R/W	00000000
220	KSV3FIFO[15:8]	7:0	KSV3FIFO Byte1	R/W	00000000
221	KSV3FIFO[23:16]	7:0	KSV3FIFO Byte2	R/W	00000000
222	KSV3FIFO[31:24]	7:0	KSV3FIFO Byte3	R/W	00000000
223	KSV3FIFO[39:32]	7:0	KSV3FIFO Byte4	R/W	00000000
224	V0[7:0]	7:0	V0 Byte0	R/W	00000000
225	V0[15:8]	7:0	V0 Byte1	R/W	00000000
226	V0[23:16]	7:0	V0 Byte2	R/W	00000000
227	V0[31:24]	7:0	V0 Byte3	R/W	00000000
228	V1[7:0]	7:0	V1 Byte0	R/W	00000000
229	V1[15:8]	7:0	V1 Byte1	R/W	00000000
22A	V1[23:16]	7:0	V1 Byte2	R/W	00000000
22B	V1[31:24]	7:0	V1 Byte3	R/W	00000000
22C	V2[7:0]	7:0	V2 Byte0	R/W	00000000
22D	V2[15:8]	7:0	V2 Byte1	R/W	00000000
22E	V2[23:16]	7:0	V2 Byte2	R/W	00000000
22F	V2[31:24]	7:0	V2 Byte3	R/W	00000000
230	V3[7:0]	7:0	V3 Byte0	R/W	00000000
231	V3[15:8]	7:0	V3 Byte1	R/W	00000000
232	V3[23:16]	7:0	V3 Byte2	R/W	00000000
233	V3[31:24]	7:0	V3 Byte3	R/W	00000000
234	V4[7:0]	7:0	V4 Byte0	R/W	00000000
235	V4[15:8]	7:0	V4 Byte1	R/W	00000000
236	V4[23:16]	7:0	V4 Byte2	R/W	00000000
237	V4[31:24]	7:0	V4 Byte3	R/W	00000000
238	Binfo[7:0]	7:0	Binfo Byte0	B/W	00000000
239	Binfo[15:8]	7:0	Binfo Byte1	B/W	00000000