CAT9883C Registers for internal

RPLLTest						
80H	R/W	7:6	00	Test Register	RPLLTest	Default Setting; Must set to 00 for proper operation.
		5	0			Smart de-Macrovision disable: Set 1 to disable smart de-Macrovision. Post-Coast is defined by register 13H
		4:0	00000			Default Setting; Must set to 00000 for proper operation.
ADC Bias Current / SOG slicer						
81H	R/W	7	0	PLL bias current test	RIPLL	Measure at Clamp pin
		6	0	ADC bias current test	RIADC	Measure at Clamp pin
		5:3	100	ADC bias current adjustment	RADCBiasI	000=40u, 001=45u, 010=50u, 011=55u, 100=60u, 101=65u, 110=70u, 111=80u
		2	0	Disable SOG slicer	REnSOGB	0=enable SOG slicer, 1=disable SOG slicer
		1	1	Tri-state SOGOUT	RTriSOGB	0=tri-state SOGOUT, 1=normal
		0	1	Tri-state VSOUT	RADCDBG	0=control via Reg[86] bit 3, 1=control via Reg[85] bit 6
ROSC / Bias-Current / Common-Voltage						
82H	R/W	6	0	ROSC test	ROSC	1=enable Ring-Oscillator output for test at Clamp pin
		5:3	100	Bias current adjust	RADCVPT	From 000 -> 111, bias current reduced
		2:0	010	Common mode voltage	RADCCMV	From 000 -> 111, common mode voltage increased
Bandwidth and Sog slicer						
83H	R/W	7:4	0000	Test Register	RINGT	Default Setting; Must set to 0000 for proper operation.
		3:2	00	Input filter bandwidth adjustment	RINBW (1 downto 0)	Input Signal Bandwidth Adjust: “00” = 300MegHz; “01” = 150MegHz; “10”=100MegHz; “11”=75MegHz; REG[86] bit2 => bandwidth area setting REG[8D] bit6 => enable signal / Active = ‘1’
		1:0	00	Sog slicer deglitch window size	RSOGBW	Default Setting; Control for bad SOG-in input. From “00” to “11”, the deglitch window is larger.
Calibration-1 (Refer REG[95H] / REG[98H])						
84H	R/W	7	0	Pixel clock source	RCK	0=internal generated, 1=from coast input
		3:2	00		R_KMode	Calibration Mode Setting: “00” for no calibration; “01” for offset calibration; “10” for white balance calibration
Data Output I/O Control						
85H	R/W	7	0	Test Register	R_422_inv	0: ROUT is UV sequence for YUV422. 1: ROUT is VU sequence for YUV422.
		6	1		RTrioutB	Data output Enable; Logic 0=Tri-State Output
Slew Rate and I/O Control						
86H	R/W	4	0	?	RVSOutLow	?
		3	1	Tristate VOut	RTriVOutB	0=put VOut in high impedance mode, 1=normal
		2	1	Input Bandwidth	RINBW(2)	0=500MHz, 1=350MHz
		1:0	10	Slew Rate	RSlew	00: Low output drive strength 01: Medium low output drive strength 10: Medium high output drive strength 11: High output drive strength
Schmitt Threshold function.						

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87H	R/W	7	0	Schmitt Type	RSMIType	0=type 0, 1=type 1
		6:4	010	Schmitt Threshold	RSMITh	111 to 000 with descending level
		3	1	HSInEn	RHSInEn	0=Disable Hsync Input; for Power down or noise reduction.
		1	0	OSCExt	ROSCExt	Test Mode: External OSC cLK
		0	1	CKMode160	RCKMode160	Test Mode: Control 160M/10M CLK TEST
Lock Threshold						
88H	R/W	6:4	001	Lock Threshold	R_PG_CHInc	Number of valid HSync for filter lockingWW
		3:0	1000	?	R_PG	?
Unlock Threshold						
89H	R/W	6:4	011	Unlock Threshold	R_PG_CHInc	Number of nonvalid HSync for filter unlocking
		3:0	0010	?	R_PG	?
Lock Windown						
8AH	R/W	7:2	000011	Lock Window	R_Fwin	Window for valid leading HSync edge (number of 40M clock)
SOG Filter and Bandwidth enable switch						
8DH	R/W	7	0	SOG Filter Bypass	RSOGFlt-Bypass	0=active, 1=bypass
		6	0	Enable Filter	REnFilt	0=disable, 1=enable [Input filter bandwith enable signal]
Clock Output Inverter						
8EH	R/W	7	0	Clock Out Inverter	RCKInv	0=no inverter, 1=inverter
Password						
8FH	R/W	7:0	00000000	Password		Password to access registers after 86H (86H is included)
Filter Control from Hsync and SOGout						
90H	R/W	7	0	Hsync filter disable	R_FWin_dis	1=disable hsync filter for PLL
		6	0	Hsync filter window type	R_FWin_Sel	
		5	0	Hsync filter reset	R_Fltr_Rst	1=reset hsync filter
		4	0		R_HVCnt_HS	0=use regenerated hsync, 1=use raw hsync for H/V counter
		3	0	sample edge of PLL lock hsync	R_PLL_HS_f	0=rising edge sample PLL lock hsync 1=falling edge sample PLL lock hsync
		2	0	SOGOUT type	R_SOGOut_Sel	0=raw sogout, 1=filtered hsync
		1:0	00	HSOUT Select	R_HSO_Sel	0X=auto select from input and PLL, 10=from input, 11=from PLL
Coast-Setting / Vsync Polarity / Hsync Check						
91H	R/W	7	0	Mode change	R_ModeChg	1=mode change
		6	0	PLL coast disable	R_Coast_dis	1=no coast for PLL
		5	1	Coast position	R_Coast_mid	1=coast falling at mid of hsync
		4:2	100	Vsync polarity detect threshold	R_VS_PD_thr	
		1:0	00	Hsync in Vsync check	R_NoHinV	0X=auto, 10=hsync in vsync period, 11=no hsync in vsync period
Hsync / Vsync Clamping						
92H	R/W	5	0	Input VSYNC sample delay	R_VSdly	0=no delay 1=delay16 clock to sample input vsync

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		4	0	Disable auto Vsync separation threshold	R_SepThr_dis	1=disable auto control of vsync separation threshold
		3	0	Clamp vs hsync edge	R_Clp_Lead	“0”=clamp from hsync trailing edge / “1”=clamp from hsync leading edge
		2:0	111	IGO hsync clamping period	R_ClpSyncDur	Clamping Duration
Clamp Enable & Dither mode & Hsync Sample						
93H	R/W	7	0	Enable Clamp (0)	R_Coast_Clp_en	0=enable clamp during coast period 1=disable clamp during coast period Disable clamp when coast
		6:4	001	Input hsync sample phase selection	R_PhSel	000=0~3, 001=4~7, 010=8~11, 011=12~15, 100=16~19, 101=20~23, 110=24~27, 111=28~31
		3:2	00	Dither mode	R_dith_mode	
		1:0	00	Dither quantity	R_dith	
PLL function-1 reg96h and reg94h						
94H	R/W	7:4	0101	Pll function		charge pump current gain
		3:2	10	Pll function		Kvco
		1	0	Pll function		set relation of cp[2:0] and charge pump current to original 9883
		0	1	Pll function		1=enable kick function as original 9883
Calibration-2 Control						
95H	R/W	5	1		R_Gain_80	1=gain/offset register all set to ‘0x80h’
		4:3	00	Gain/Offset calibration option	R_KRdyOpt	
		2	0	Calibration date average type	R_KAver_opt	
		1:0	10	Offset target code	R_OTC	00=0 LSB, 01=1 LSB, 10=2 LSB, 11=4LSB
PLL function-2 & SOG noise reduction						
96H	R/W	5	1	VSYNC I/O enable	R_VSYN_EN	0=disable vsync IO input, 1=enable vsync IO input
		4	0	Reduce SOG input noise	R_SOGNR	0=default, 1=enable SOG input noise reduction
		3	0	Pll function		1=disable extra ring osc load cap
		2	0	Pll function		1= normal size charge pump for external loop filter
		1	1	Pll function		1=enable external filter
		0	0	Pll function		1=disable internal digital damping filter
?						
97H	R/W	4	0	Test mode for cal	R_Test_K	
		3:0	0101	IGO target code	R_YTC	96+(0~15)x2
Calibration-3						
98H	R/W	7	0	Calibration type	R_K1	0=background calibration, 1=one time calibraion
		6	0	IGO enable	R_KY	0=disable IGO, 1=enable IGO
		5:4	01	Calibration update frequency	R_KFreq	00=16 hsync, 01=32 hsync, 10=64 hsync, 11=1 vsync

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		3:2	10	IGO cycles	R_YLoop	00=1 cycles, 01=2 cycles, 10=3 cycles, 11=4 cycles
		1:0	01	One time calibration cycles	R_Loop	00=16 cycles, 01=32 cycles, 10=64 cycles, 11=128 cycles
Pattern Gen & Others and Calibration-4						
99H	R/W	7	0	Pattern Gen enable	R_PG_En	1=enable pattern generator output
		6	0	Pattern Gen mode	R_PG_Mode	
		5:4	00	Gain/Offset hold	R_KHold	00=no hold, 01=hold offset, 10=hold gain, 11=hold gain/offset
		3	1	Ready for Gain/Offset calibration	R_KRdy	1=ready to do gain/offset calibration
		2	0	Test mode	R_TestMode	
		1	0	Ring OSC source	R_Clk40m_sel	?
		0	0	External Clock	R_Clkpix_sel	Enable Coast input signal that output on output I/O clock pin.
Read Only Values (Others)						
A0H	R	4:0				PLL_Lock&FLock&KS;
A1H	R	7:0		R offset code	O1_r	When R gain=0x80
A2H	R	7:0		G offset code	O1_g	When G gain=0x80
A3H	R	7:0		B offset code	O1_b	When B gain=0x80
A4H	R	7:0		R offset code	O2_r	When R gain!=0x80
A5H	R	7:0		G offset code	O2_g	When G gain!=0x80
A6H	R	7:0		B offset code	O2_b	When B gain!=0x80
A7H	R	7:0		R gain code	G_r	
A8H	R	7:0		B gain code	G_b	
A9H	R	7:0		IGO calibration code	Y_g	
ACH	R	3:0		12bits Hsync period by system clock		regach<=VLine(11 downto 8)&HPer(11 downto 8);
AAH	R	7:0				regaah<=HPer(7 downto 0);
ACH	R	7:4		12bits Vertical line number		regach<=VLine(11 downto 8)&HPer(11 downto 8);
ABH	R	7:0				regabh<=VLine(7 downto 0);